PRIAM

# FOURTEEN INCH WINCHESTER DISK DRIVES

# OEM/SERVICE MANUAL

MARCH 15, 1982

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P R E L I M I N A R Y

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REVISED September 20, 1982

# PRIAM

# 14-INCH WINCHESTER DISC DRIVES

# FIELD SERVICE MANUAL

MARCH 15, 1982

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P R E L I M I N A R Y

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**PREFACE**

This manual has been prepared for the benefit of field service personnel who are directly involved with the installation and maintenance of PRIAM 14-inch disc drives. It may also contain information helpful to the OEM manufacturer of products containing these drives.

In producing this manual, PRIAM has sought to provide enough information to enable the following field operations to proceed smoothly and efficiently:

Preparation, including provision for compatibility of related equipment, proper power, and cabling.

Installation and initial testing.

Fault isolation to the assembly level.

Assembly replacement.

The manual contains enough theory of operation to give the reader a general background on how the drive works. This is intended solely to provide a context for the testing and troubleshooting procedures. It is not intended that the manual should enable the reader to do detailed intra-board troubleshooting or board repair.

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# SECTION 1 - GENERAL INFORMATION

PRIAM 14-inch Winchester disc drives are available in three models, providing a range of storage capacities, as shown in the following table:

| Model Number | Megabytes | Discs | Data Heads | Tracks/Inch |
|---|---|---|---|---|
| DISKOS 3350 | 34 | 1 | 3 | 480 |
| DISKOS 6650 | 68 | 1 | 3 | 960 |
| DISKOS 15450 | 158 | 2 | 7 | 960 |

## 1.1 FEATURES

The advantages offered by the 14-inch family of disc drives include:

1. High Storage Capacity
2. Low Cost per Megabyte
3. High Performance
4. High Reliability
5. Relatively Small Size
6. Universal Power Compatibility
7. Ease of Interfacing

The above advantages are achieved through a combination of design features, as described in the following paragraphs:

1. High storage capacity is achieved by using the larger (14") disc size, in conjunction with high recording and track densitites.
2. Low cost per megabyte is achieved by using efficient and cost-effective methods throughout the entire design, manufacturing, and marketing process.
3. High performance is achieved through the use of fully servoed, linear voice coil head positioning. This makes possible the high precision and stability needed in order to utilize the higher recording and track densities. It also enables the fast access times necessary for efficient use of the larger data bases.
4. High reliability is achieved through the use of a fully sealed, positive pressure air filtering system, servoed spindle speed and head positioning systems, cast metal head disc assembly, efficient cooling system, and microprocessor implementation of control functions.

5. Overall size is kept small by designing the various assemblies in the proper relationships to one another. The (optional) power supply is designed so that it can fit inside the standard frame. Thus a PRIAM 14-inch disc drive with the power supply included does not require much more space than a standard size 8-inch drive with a separate power supply. All three drives in the PRIAM 14-inch family have identical overall dimensions. Standard rack mounting can be used.

6. Power compatibility is assured through the use of all DC components, including a DC spindle motor. Even when the built in power supply option is selected, PRIAM drives can still be used anywhere in the world, since the power supply input can be strapped to accomodate any of the prevailing line voltages.

7. Ease of interfacing is assured by the availability of several different interfaces, including a PRIAM standard interface, a PRIAM SMD interface, and an ANSI interface. Each of these has been designed in relation to an entire class of existing computer hardware. Virtually any bus now in use can be accomodated by one PRIAM interface or another. See the section on Options (below) for a complete listing.

## 1.2 SPECIFICATIONS

Table 1.2-1 summarizes the operating characteristics, physical characteristics, and power requirements for the three drives in the PRIAM 14-inch family.

## 1.3 CONFIGURATION

### 1.3.1 Physical Configuration

Figure 1.3-1 shows the overall physical configuration for the DISKOS 3350, 6650, or 15450.

### 1.3.2 Functional Organization

Figure 1.3-4 is a simplified block diagram showing the relationships among the major functional units in a PRIAM 14-inch disc drive.

Table 1.2-1. Specifications for PRIAM 14-inch Disc Drives

OPERATING CHARACTERISTICS

| | DISKOS 3350 | DISKOS 6650 | DISKOS 15450 |
|---|---|---|---|
| Capacity (unformatted) | 33.9 Mbytes | 67.8 Mbytes | 158.2 Mbytes |
| Transfer rate (megabytes/second) | 1.04 | 1.04 | 1.04 |
| Track-to-track seek time (typical) | 8 msec | 8 msec | 8 msec |
| Average seek time (typical) | 45 msec | 45 msec | 40 msec |
| Maximum seek time (typical) | 85 msec | 85 msec | 75 msec |
| Average latency | 9.7 msec | 9.7 msec | 9.7 msec |
| Tracks per inch | 480 | 960 | 960 |
| Bits per inch | 6430 | 6430 | 6430 |
| Number of data surfaces | 3 | 3 | 7 |
| Number of data cylinders | 561 | 1121 | 1121 |
| Nominal RPM | 3100 | 3100 | 3100 |
| Bytes per track | 20,160 | 20,160 | 20,160 |

POWER REQUIREMENTS

Power requirements are the same for all three drives:

| | Maximum | Typical |
|---|---|---|
| + 24 VDC (±5%) | 7.0 A | 6.0 A seeking<br>4.5 A non-seeking |
| + 5 VDC (±5%) | 4.0 A* | 1.5 A |
| - 5 VDC (±5%) | 2.0 A | 1.0 A |
| - 12 VDC (±5%) | 0.7 A | 0.5 A |

* 6.0 A maximum with adapters

DIMENSIONS

Physical dimensions are the same for all three drives:

| | |
|---|---|
| Height | 6.9 inches |
| Width | 16.6 inches |
| | 17.6 inches with slides |
| Depth | 20.0 inches |
| Weight* | 52 pounds (3350 and 6650) |
| | 55 pounds (15450) |

* Includes 18 pounds for power supply. Add 6 pounds for slides.

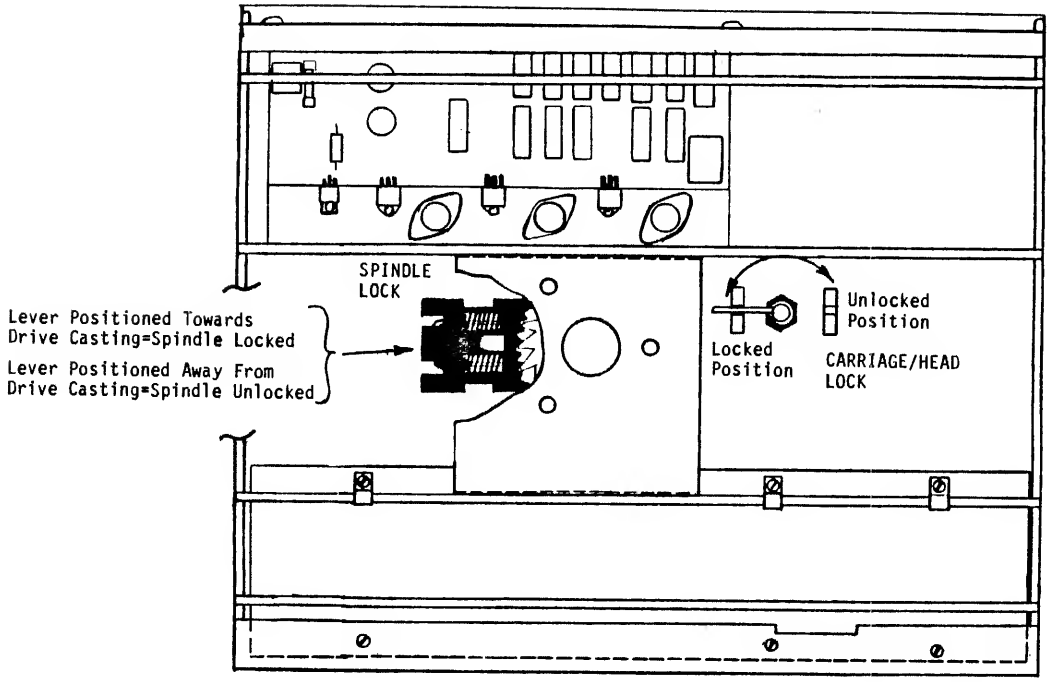



Figure 2.8-1. Location of Head and Spindle Locks

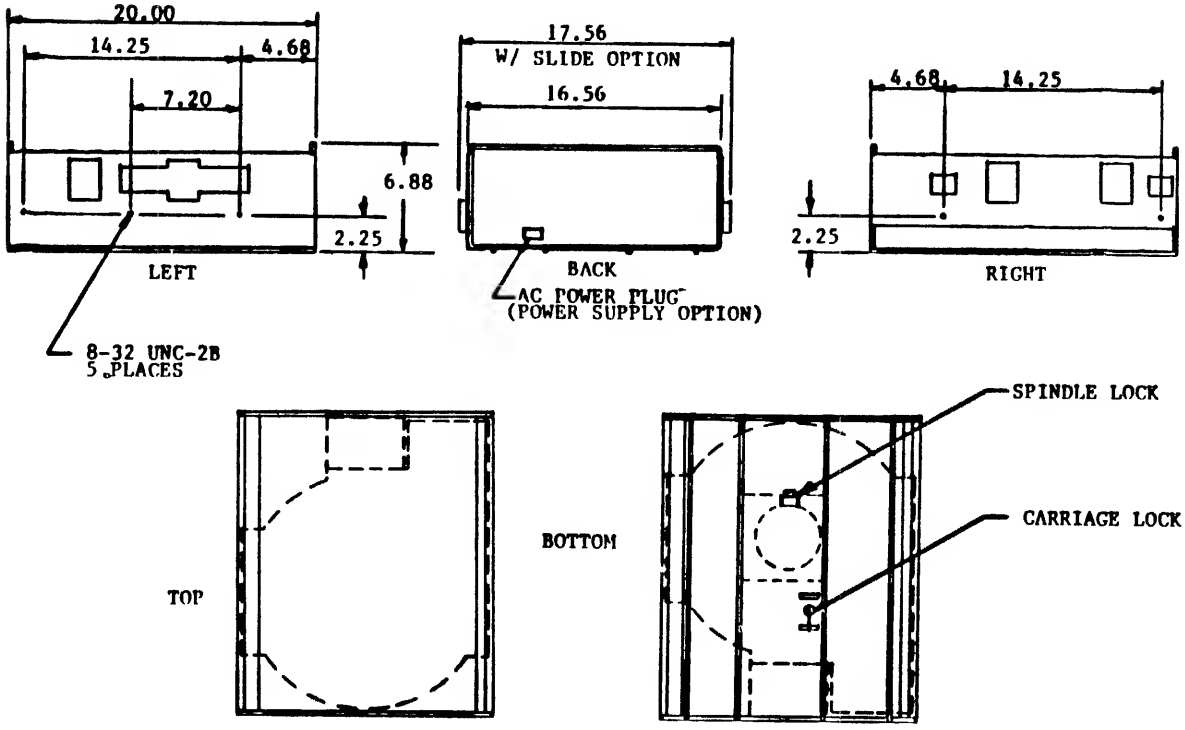
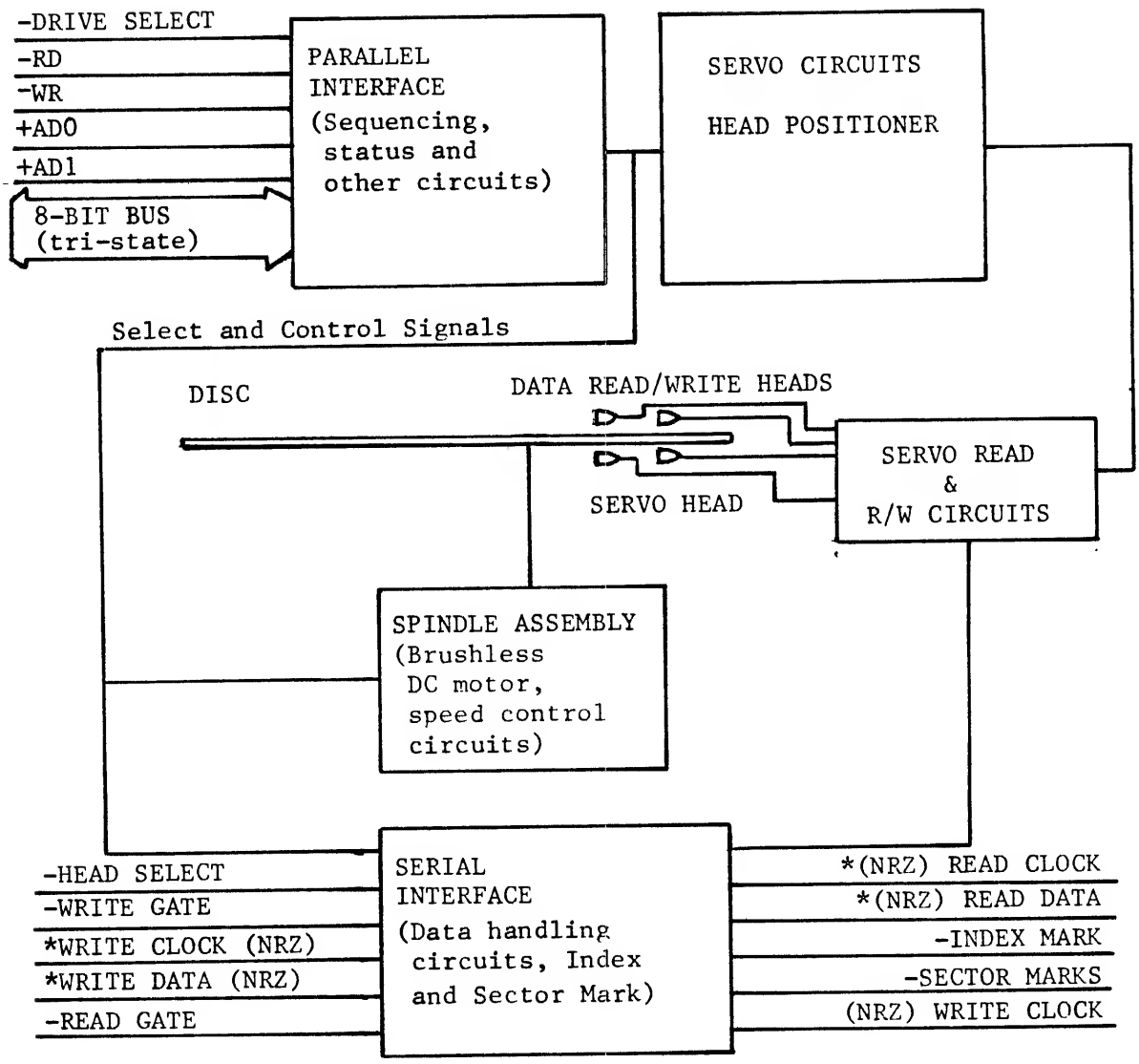



Figure 1.3-1. Physical Configuration of a PRIAM 14-inch Disc Drive




*designates differential signals.

Figure 1.3-2. Simplified Block Diagram of a PRIAM 14-inch Disc Drive

## 1.4 OPTIONS

### 1.4.1 Interface Options

The PRIAM 14-inch disc drives are available with a variety of interface options. Each of these interface options can be used, without modification, on any disc drive in the 14-inch family. All PRIAM interfaces include on-board data separation.

The standard PRIAM Interface is designed for low cost and for efficient use with microprocessor-based systems. Up to four drives may be daisy-chained, when this interface is used. The PRIAM interface provides a basic 8-bit bidirectional bus, which may be used with the currently popular 8-bit and 16-bit microprocessors. It also provides bit-serial NRZ data exchange. No elaborate handshaking protocols are required. The PRIAM interface is built into the disc drive's main PCB. A 50-conductor flat ribbon cable is used between the PRIAM interface and the host system. See the PRIAM INTERFACE section for more details.

The SMD Interface permits a PRIAM drive to be used with existing Storage Module Drive (SMD) controllers. In the 14-inch drives the SMD interface is built into the disc drive's main PCB. The line drivers and line receivers in the SMD interface are matched to those of typical SMD controllers. There are two interface cables between the host system's SMD controller and the PRIAM disc drive's SMD interface -- a 60-conductor twisted-pair flat cable ("A" cable) and a 26-conductor flat ribbon cable ("B" cable). See the SMD INTERFACE section for more details.

The ANSI Interface complies with the disc drive interface standard proposed by ANSI Technical Committee X3T9. Characteristics of the ANSI interface include variable and fixed sector sizes, data transfer rates up to 10 megabits per second, and radial attention and select capability. Up to eight drives may be daisy-chained, on a single 50-conductor flat ribbon cable. See the ANSI INTERFACE section for more details.

### 1.4.2 Interface Cables and Terminators

I/O cables are available from PRIAM, for connecting the user's controller to the PRIAM disc drive, and for connecting daisy-chained drives to one another.

Terminators are available for I/O signal lines, to minimize reflections and to ensure maximum data integrity. One set of terminators is required for a single drive, or for the base drive in a daisy chain.

### 1.4.3 Power Supplies and Cables

PRIAM's optional power supply allows PRIAM disc drives to operate from 100, 120, 220, and 240 VAC, 50 or 60 Hz power. The optional power supply is delivered already mounted within the drive frame. No extra space or interconnection is required.

### 1.4.4 Mounting Hardware

Optional slides are available from PRIAM. These slides allow easy access to drives mounted in standard racks and cabinets.

# SECTION 2 - INSTALLATION

The disc drive is packaged to withstand normal handling in a reusable shipping container. It is the customer's responsibility to notify the carrier if shipping damage should occur to the drive. Any insurance protection is also the customer's responsibility.

When the shipment is received, the shipping container should be examined for obvious signs of shipping damage. Most insurance adjusters require an inspection of the damaged container. Notify the carrier and PRIAM Customer Service immediately, if shipping damage is discovered.

## 2.1 UNPACKING

The disc drive is shipped with an outer and an inner carton. Open the outer carton by cutting the tape on the top side. Remove the inner carton and open it by cutting the tape.

Remove the disc drive from the carton and place it on a clean, flat work surface. Remove the wrap.

## 2.2 VISUAL INSPECTION

Visually inspect the drive for loose, bent, or broken parts. Report any damage to the carrier and to PRIAM Customer Service.

## 2.3 POWER SUPPLY SETUP

If a PRIAM optional power supply is present, check the AC voltage selection circuit board prior to applying power. This board is adjacent to the AC input plug, and is an integral part of the power supply. To select a voltage, remove the selection circuit board and reinsert it so that the proper AC voltage designation (100, 120, 220, or 240) is visible. Also check the fuse value. A 5 ampere fuse is used with 100 or 120 VAC, while a 2.5 ampere fuse is used with 220 or 240 VAC. No modification is required for changing from a 60 Hz power source to a 50 Hz power source, or vice versa.

## 2.4 SWITCH SETTINGS

The drive address, write protect parameters, and sector size are all switch selectable. The switches are located on the main PCB. Referring to Figures 2.4-1, 2.4-2, and 2.4-3, and to Table 2.4-1, set the switches according to the desired operating conditions.

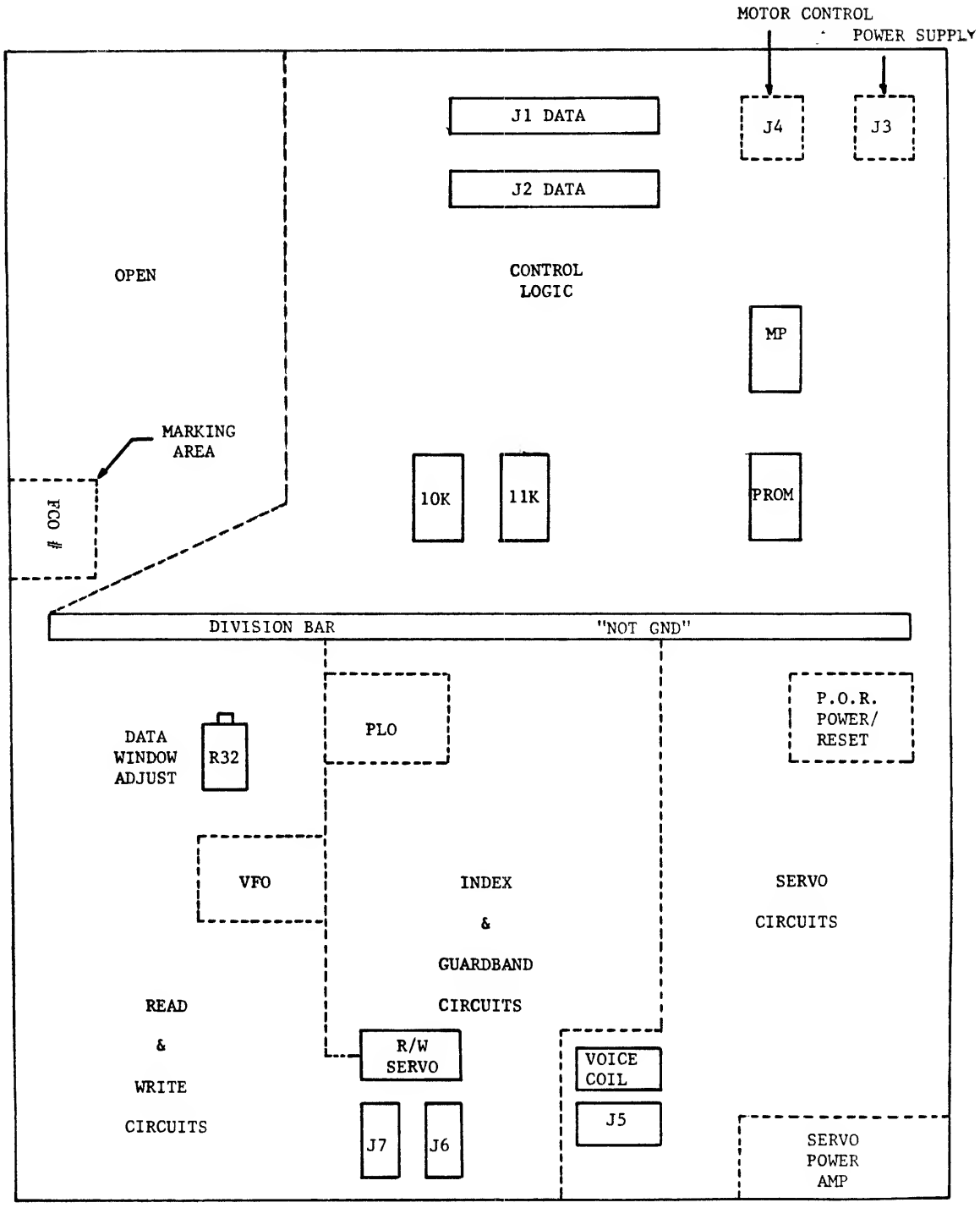



Figure 2.4-1. Main PCB (PRIAM Interface, "B" Drive)

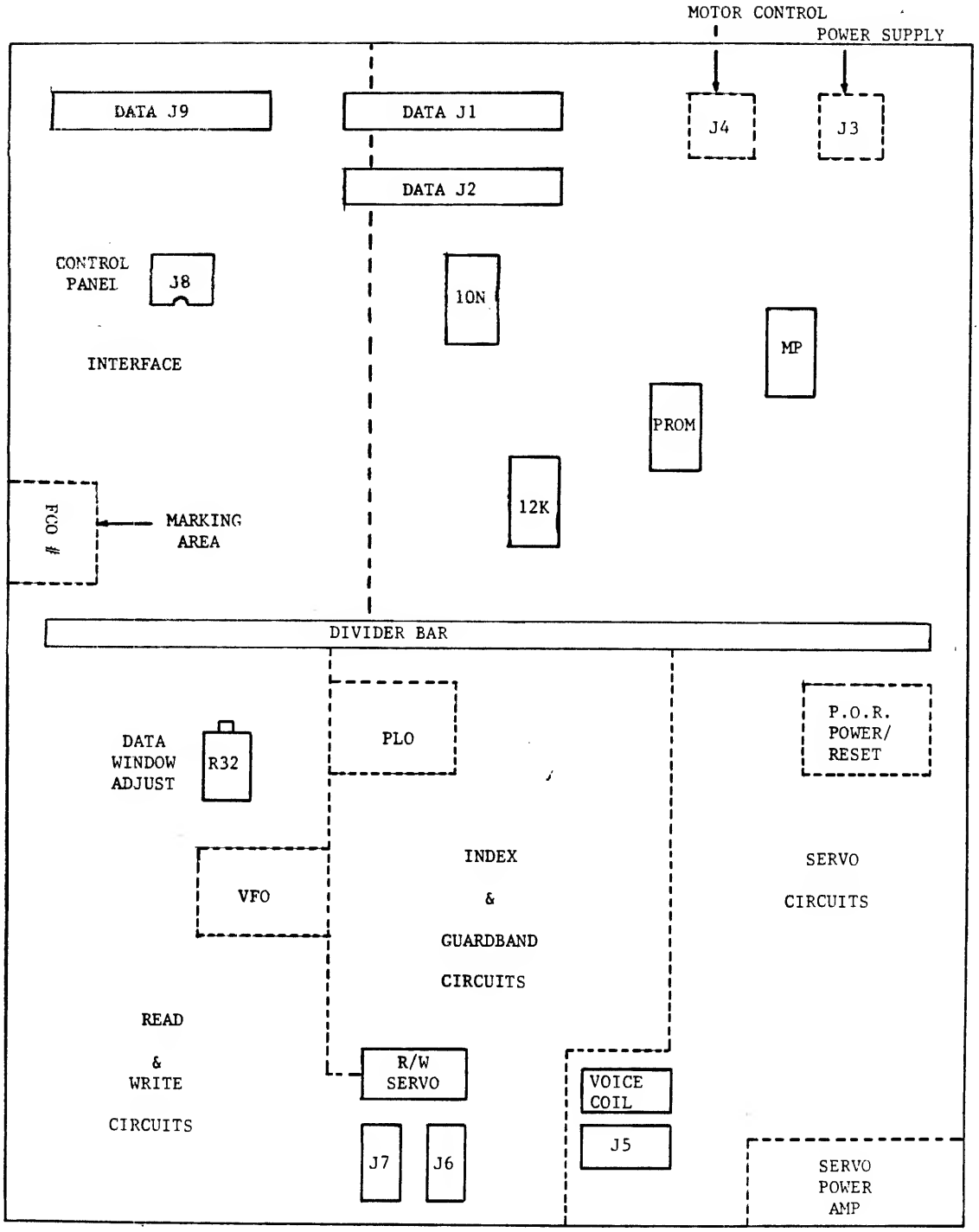



Figure 2.4-2. Main PCB (SMD Interface)

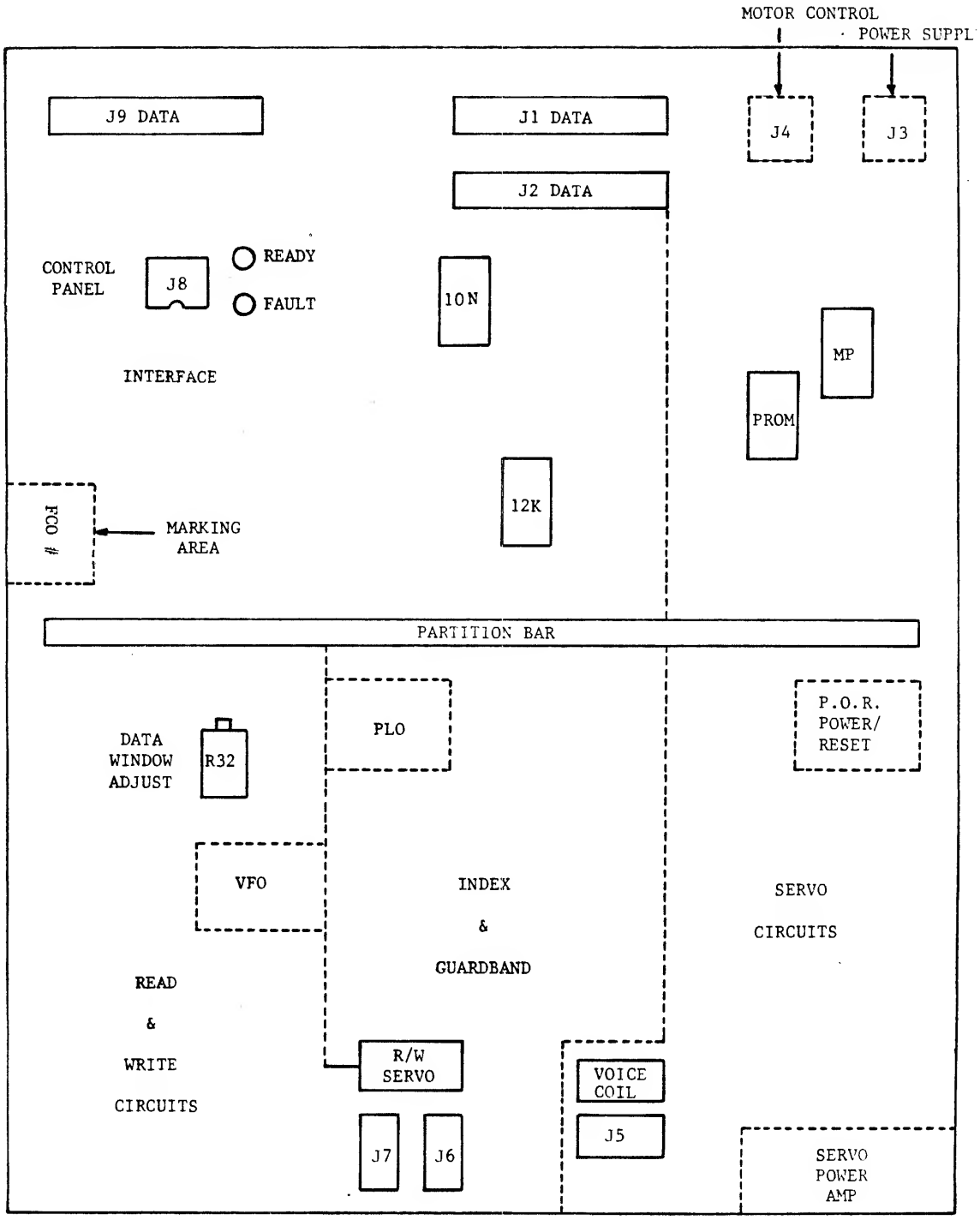
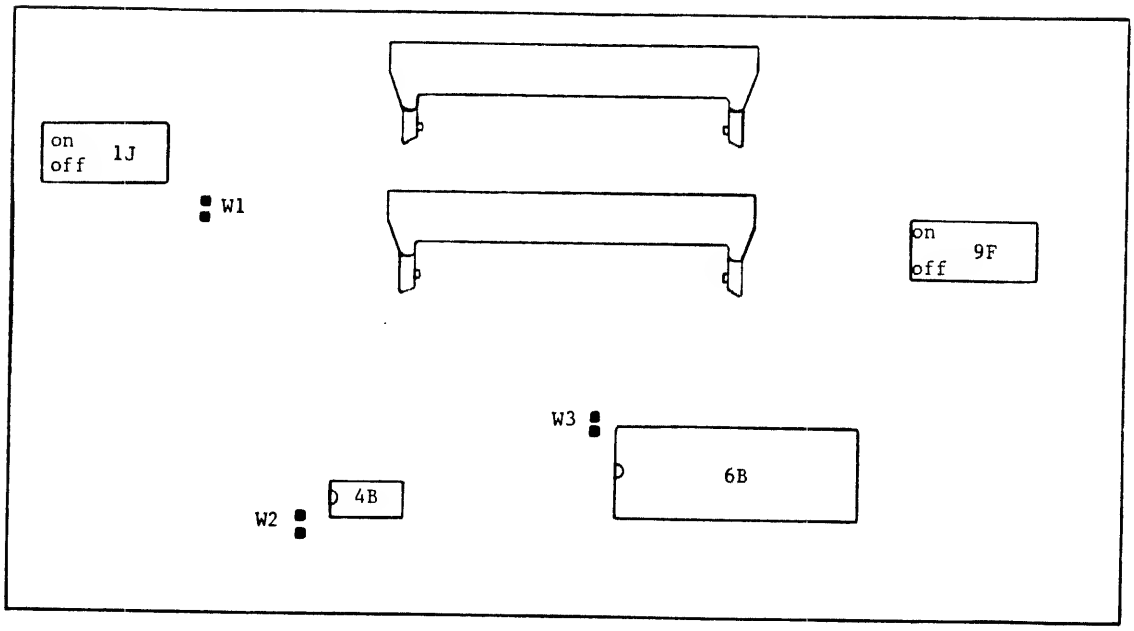
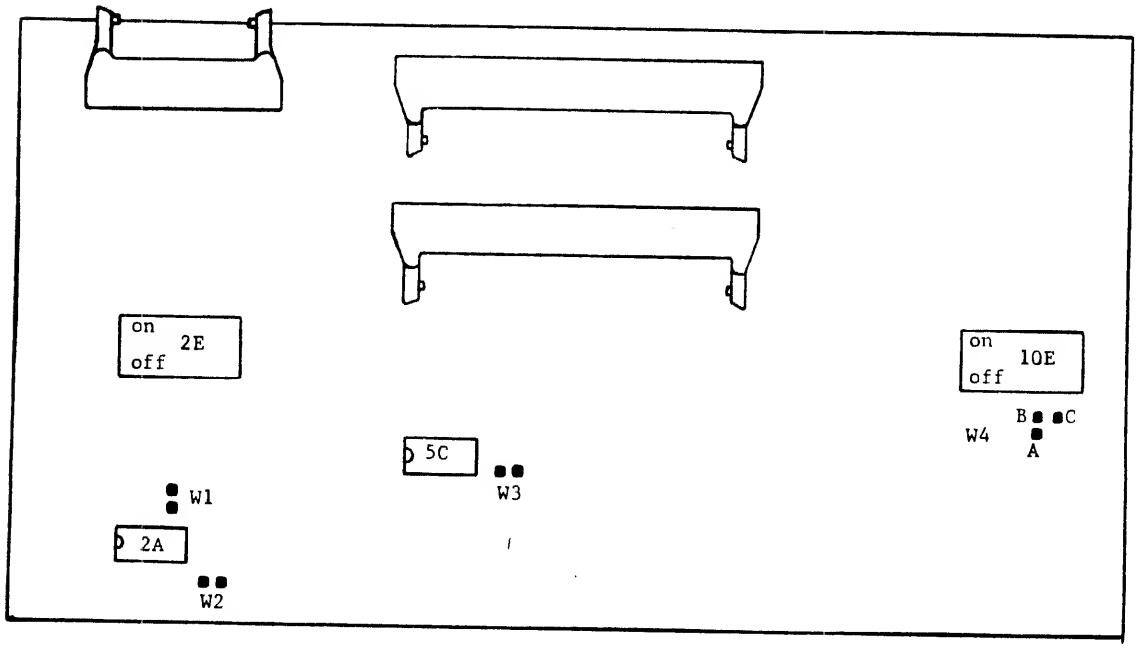



Figure 2.4-3. Main PCB (B-4 Interface)

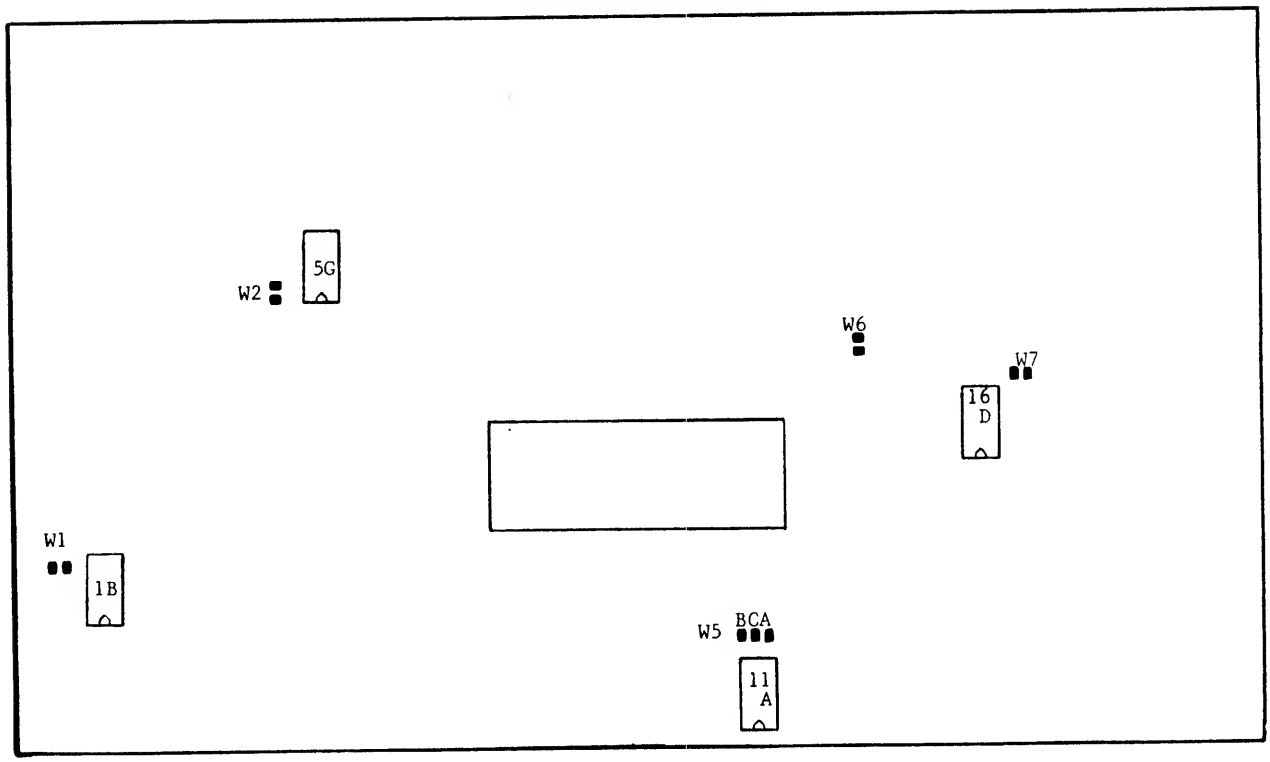
15450 SPLIT PRIAM 200208




15450 SPLIT SMD 200218 & 200263



15450 Split Analog PCB 200213




| SWITCH LOCATION | 15450-10 1J NUMBER/FUNCTION | 15450-20 2E NUMBER/FUNCTION |
|---|---|---|
| 1 | DEVICE SELECT 1 | DEVICE SELECT 1 |
| 2 | 2 | 2 |
| 3 | 3 | 4 |
| 4 | 4 | 8 |
| 5 | | |
| 6 | | |
| 7 | | |
| 8 | . | ON=WRITE PROTECT |

| SWITCH LOCATION | 9F NUMBER/FUNCTION | 10E NUMBER/FUNCTION |
|---|---|---|
| 1 | 1 | 16 |
| 2 | 2 | 32 |
| 3 | 4 | 64 |
| 4 | 8 | 128 |
| 5 | 16 | 256 |
| 6 | 32 | 512 |
| 7 | 64 | 1024 |
| 8 | OFF=SECTOR/TRACK ON=BYTES/SECTOR | OFF=SECTOR/TRACK ON=BYTES/SECTOR |

Table 2.4-1. Switch Settings on the Main PCB

"B" Level Drive with PRIAM Interface

| Switch # in Group | Switch Group Location on PCB | |
|---|---|---|
| | 10K | 11K |
| 1 | Drive Select 1 | 1 sector/track<br>16 bytes/sector |
| 2 | Drive Select 2 | 2 sectors/track<br>32 bytes/sector |
| 3 | Drive Select 3 | 4 sectors/track<br>64 bytes/sector |
| 4 | Drive Select 4 | 8 sectors/track<br>128 bytes/sector |
| 5 | Skip Defect Prot.<br>On = Protected | 16 sectors/track<br>256 bytes/sector |
| 6 | Write Enable<br>All Heads | 32 sectors/track<br>512 bytes/sector |
| 7 | Write Clock<br>Off=Open<br>On=Closed | 64 sectors/track<br>1024 bytes/sector |
| 8 | Write Clock<br>Off=Normal<br>On=Inverted | See Note Below |

Note: When Switch 8 is Off, Switches 1-7 select sectors/track.
When Switch 8 is On, Switches 1-7 select bytes/sector.

SMD Interface

| Switch # in Group | Switch Group Location on PCB | |
|---|---|---|
| | 10N | 12K |
| 1 | Drive Select 1 | 1 sector/track |
| 2 | Drive Select 2 | 2 sectors/track |
| 3 | Drive Select 4 | 4 sectors/track |
| 4 | Drive Select 8 | 8 sectors/track |
| 5 | Reserved | 16 sectors/track |
| 6 | Reserved | 32 sectors/track |
| 7 | Reserved | 64 sectors/track |
| 8 | Write Protect<br>All Heads | Off |

24W 16K
2048 2
1024 1
512 WRT EN & OFF PROT
256
128 4
64 3
32 2
16 DS1

| | | MODEL NUMBER | | | | | |
|---|---|---|---|---|---|---|---|
| | | 3350-10 | | 6650-10 | 3350-20 | | 6650-20 |
| PCBA NUMBER | | 200173-01 | 200113 | 200173-02 | 200088 | 200148-01 | 200148-02 |
| NOTE 1: ON THIS PRODUCT GROUP NO USER FUNCTIONS ARE JUMPER SELECTABLE. THIS CHART IS FOR REFERENCE ONLY. NOTE 2: * INDICATES NO A-B OR B-C OPTION. | W1 | * | * | * | * | B-C | A-B |
| | W2 | * | * | * | * | * | * |
| | W3 | * | * | * | * | * | * |
| | W4 | * | * | * | * | * | * |
| | W5 | * | * | * | * | B-C | B-C |
| | W6 | A-B | * | B-C | * | * | * |
| | W7 | * | * | * | * | * | * |
| | W8 | A-B | * | B-C | * | * | * |
| | W9 | * | * | * | * | * | * |
| | W10 | * | * | * | * | * | * |
| | W11 | A-B | | B-C | | A-B | B-C |
| | W12 | B-C | | A-B | | B-C | A-B |
| | W13 | * | | * | | A-B | B-C |
| | W14 | * | | * | | A-B | B-C |
| | W15 | A-B | | B-C | | A-B | B-C |
| | W16 | A-B | | B-C | | B-C | A-B |
| | W17 | A-B | | B-C | | INSTALLED | OPEN |

| | | MODEL NUMBER | |
|---|---|---|---|
| | | 15450-10 | 15450-20 |
| PCBA NUMBER | | 200208 | 200218/200263 |
| JUMPER NUMBER AND FUNCTION (When Jumper is IN) | W1 | WRITE PROTECT | "OR INDEX & SECTOR WITH READ GATE |
| | W2 | SKIP DEFECT RECORD NOT PROTECTED | ENABLE ADDRESS MARK |
| | W3 | ENABLE LONG RESET | AUTO SEQUENCE UP |
| | W4 | | A-B ENABLES CYLINDER ADDRESS BIT 10<br>B-C DISABLES BIT 10 |

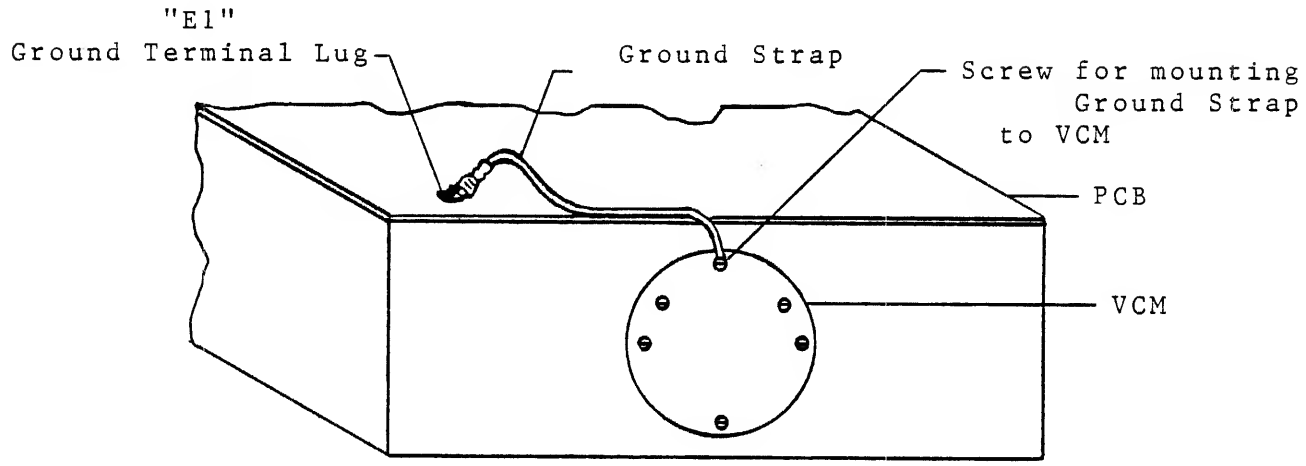
JUMPER SELECTION CHART

15450 Analog Split 200213 W1,W2,W6 & W7 Installed; W5 B-C position;

## 2.5 MOUNTING

The disc drive may be mounted in a standard 19-inch rack. If the optional slides are present, they may be installed at this time.

## 2.6 GROUNDING




## 2.7 CABLING

If a separate power supply is used, the power cable should be installed to connector J3 on the Main PCB. The DC voltages required at the respective pins on J3 are listed (below) in the PERFORMANCE CHECK section. Interface cables to the host system are described in the sections covering each of the available interface options. Cabling between assemblies within the disc drive is completed at the factory prior to shipment. More details on inter-assembly cabling are given in the ASSEMBLY REPLACEMENT PROCEDURES section.

## 2.8 UNLOCKING

Both the drive spindle and the head carriage are locked prior to shipment. After the drive has been completely mounted and cabled, these must be unlocked to enable normal operation.

The spindle lock and the head carriage lock are both fully accessible on the bottom of the HDA (Head Disc Assembly). Referring to Figure 2.8-1, place both levers in the UNLOCK position.

**CAUTION: AVOID MANUAL ROTATION OF THE SPINDLE OR MOVEMENT OF THE CARRIAGE. DAMAGE TO THE DISC SURFACE MAY OCCUR IF THE HEADS ARE MOVED ACROSS A NON-ROTATING DISC SURFACE.**

## 2.9 PERFORMANCE CHECK

Conduct a performance check, as described in the OPERATING PROCEDURES section.

## 2.10 LOCKING

Both the drive spindle and the head carriage should be locked whenever the drive is to be physically moved, even if it is not to be shipped. To lock the drive, refer to Figure 2.8-1, and place both levers in the LOCK position.

## 2.11 REPACKING

Repacking is the reverse of the unpacking procedure. Prior to repacking the drive, make sure that the spindle and carriage locks are in the LOCK positions.

## 2.12 STORAGE

When the environment is severe, or when the drive is to be stored for a long time, it should be repacked prior to storage.

When storing unpacked drives, avoid dusty or unstable environments.

## 2.13 SHIPPING

Contact PRIAM Customer Service for a return authorization number prior to shipping a drive or assembly to PRIAM. After locking the drive spindle and head carriage, pack the drive in its original carton or an equivalent one.

# SECTION 3 - OPERATING PROCEDURES

## 3.1 SPINDLE AND HEAD LOCKS

Before the drive can be operated, it is necessary to place both spindle and head lock levers in the UNLOCK position. Refer to Figure 2.8-1 for the locations of these levers.

**Whenever the drive is to be moved for any reason, the spindle and head lock levers should both be placed in the LOCK position.**

## 3.2 POWERING UP/DOWN

The exact procedure for powering up the drive depends on the interface option present.

If the drive has a standard PRIAM interface, apply DC power, select the drive (via the -DRIVE SELECT lines) and issue a Sequence Up command.

If the drive has an SMD interface, apply DC power, select the drive (via the UNIT SELECT lines), then bring PICK and HOLD to ground.

If the drive has an ANSI interface, apply DC power, select the drive (via the Attn / Select lines, then issue a Spin Up command.

If the drive has a BASIC FOUR interface, apply DC power and select the drive (via the UNIT SELECT lines).

Similarly, the procedure for powering down also depends on the interface option present:

If the drive has a standard PRIAM interface, issue a Sequence Down command.

If the drive has an SMD interface, remove the ground from PICK or HOLD.

If the drive has an ANSI interface, issue a Sequence Down command.

If the drive has a BASIC FOUR interface, remove DC power.

## 3.3 PERFORMANCE CHECK

The following procedures are recommended as an initial check for proper operation of the disc drive:

1. Check the DC voltage levels (J3 on the main PCB).

| Voltage | J3 pin # | Tolerance |
|---|---|---|
| GND | 1 | N/A |
| +24 VDC | 2 | ±5% running<br>+5%-15% at spindle startup |
| -5 VDC | 3 | ±5% |
| -12 VDC | 4 | ±5% |
| +5 VDC | 5 | ±5% |
| 24 V RETURN | 6 | N/A |

2. If any voltages are outside specification, check the corresponding current demands.

| Voltage | Maximum Current |
|---|---|
| -5 VDC | 2.0 amperes |
| +5 VDC | 4.0 amperes for 3350 drive<br>6.0 amperes for 6650 drive<br>6.0 amperes for 15450 drive |
| -12 VDC | 0.7 amperes |
| +24 VDC | 7.0 amperes from start of spindle rotation until Ready.<br>5.0 amperes after Ready.<br>6.0 amperes after Ready during an active seek operation. |

3. Power up the drive, as detailed in the POWERING UP/DOWN section, above. Spindle rotation should begin.

4. Watch for the drive to become Ready. If no faults are detected during the power up sequence, this will take about 60 seconds. If a fault is detected (by the safety circuits within the drive), Ready will be inhibited and a fault condition will be reported. See the STATUS AND ERROR CODES section of the TROUBLE SHOOTING PROCEDURES for details. If, after two minutes, the microprocessor within the drive is unable to sense that the spindle is rotating at the specified speed, Ready will be inhibited and spindle rotation will stop.

5. Check the head positioning operation by issuing seek commands. The following seek pattern is suggested:

   From 000 to 001 to 000 to 002 to 000 to 003 to 000 to 004 to 000 to 005 to 000 ... to maximum cylinder address.

6. Verify that the average seek time complies with the specification. This is done by performing a seek between cylinder 000 and a specified "average" cylinder, and watching for an indication that the seek has been completed. The cylinder number and the maximum time allowed both depend on the disc drive type. The signal line to be monitored depends on the interface type. The following table gives details:

| Drive Type | Cylinder # | Seek Time |
|---|---|---|
| DISKOS 3350 | 187 | 45 msec |
| DISKOS 6650 | 374 | 48 msec |
| DISKOS 15450 | 374 | 45 msec |

| Interface Type | Signal Line Monitored |
|---|---|
| Standard PRIAM | -READY |
| SMD | ON CYLINDER |
| ANSI | BUSY |
| BASIC FOUR | ON CYLINDER |

7. Check for proper data transfer operation by writing and then reading data with each read/write head.

   **CAUTION: WRITE OPERATIONS ALTER PREVIOUSLY RECORDED DATA**

   Most disc systems require a formatted disc before data transfer can be performed.

   A disc surface defect map is supplied by PRIAM with each disc drive. The defect map indicates the location of defects discovered during manufacturing and testing. A defect location is specified by the number of byte positions from the index mark.

# SECTION 4 - ASSEMBLIES

## 4.1 OVERVIEW

PRIAM disc drives are constructed in a modular fashion, so that defective assemblies can be easily replaced. This greatly reduces down time due to servicing. The six assemblies are:

Head Disc Assembly

Photocell Assembly

Motor Control Assembly

Main PCB

Power Supply

Frame Assembly

The exact procedures for removing and replacing these assemblies are described in the ASSEMBLY REPLACEMENT PROCEDURES section.

## 4.2 HEAD DISC ASSEMBLY

The Head Disc Assembly (HDA) is a contamination-resistant enclosure. It contains the drive spindle assembly, drive motor, voice coil actuator, head carriage assembly, read/write heads, magnetic disc(s), and air filter assemblies.

## 4.3 PHOTOCELL ASSEMBLY

The Photocell Assembly contains three infrared light-emitting diodes and phototransistors. Its purpose is to monitor and control spindle motor rotation.

## 4.4 MOTOR CONTROL ASSEMBLY

The Motor Control Assembly contains the circuitry associated with driving the spindle motor. This circuitry receives an On/Off command from the Main PCB, and spindle rotation feedback from the Photocell Assembly.

## 4.5 MAIN PCB

The main PCB contains all the circuitry associated with head positioning, read/write control, command execution, and information transfers across the user interface.

## 4.6 POWER SUPPLY

If the PRIAM power supply option is chosen, the power supply is mounted within the Frame Assembly. The PRIAM power supply can operate from 50 or 60 Hz, with input voltage (selectable) of 100, 120, 220, or 240 VAC.

## 4.7 FRAME ASSEMBLY

The Frame Assembly is constructed to accomodate all of the standard and (PRIAM-built) optional assemblies of the disc drive. Its open steel rod and sheet metal design provides improved air circulation, and also makes the drive lighter, lower in cost, and easier to install.

# SECTION 5 - FORMATS

## 5.1 OVERVIEW

The PRIAM 3350 disc drive has a single disc with two magnetic surfaces. Each surface accomodates two heads, as shown in Figure 5.1-1. On the "bottom" surface, the inner head reads the servo information, and the outer head writes and reads data surface 0. On the "top" surface the outer head writes and reads data surface 1, and the inner head writes and reads data surface 2.

The PRIAM 6650 has exactly the same configuration of disc surfaces and heads as the 3350, but it achieves twice the storage capacity by having twice as many tracks per inch.

The PRIAM 15450 has two discs. The configuration of the "lower" disc is exactly like that of the disc on the 6650. The "upper" disc has four data heads, which write and read data surfaces 3 through 6.

## 5.2 SERVO SURFACE -- NON-QUADRATURE

The purpose of the servo surface is to provide a coordinate system by means of which the electrical circuitry of the disc drive can locate specific areas for writing or reading data. The servo surface itself is written once at the factory, and thereafter is a read-only area. The information on the servo surface is used to determine the angular position of the disc, as well as the radial position of the head carriage.

The servo surface for the 3350 is divided into four distinct groups of tracks. From the inside (hub) out, these are as follows:

a. Guardband 3 - 22 tracks

b. Servo data band -

c. Guardband 1 - 7 tracks

d. Guardband 2 (landing zone) - 45 tracks

Within each of these bands, there are two types of tracks -- odd tracks and even tracks. Each track type produces a characteristic signal at the read head, as described below in the **SERVO PATTERN** section. If the read head is closer to an odd track, the odd pattern will have greater amplitude. In the same manner, the even pattern will have greater amplitude if the read head is closer to an even track.

The servo circuitry compares the amplitudes of the signals from the adjacent tracks, and identifies the equal-amplitude condition as a "track crossing". During seek operations, the servo circuitry counts the track crossings in order to derive the cylinder address of the data write/read heads. During write and read operations, the servo circuitry adjusts the position of the head carriage in such a manner as to preserve the equal-amplitude condition, thus keeping the write/read head "on track".

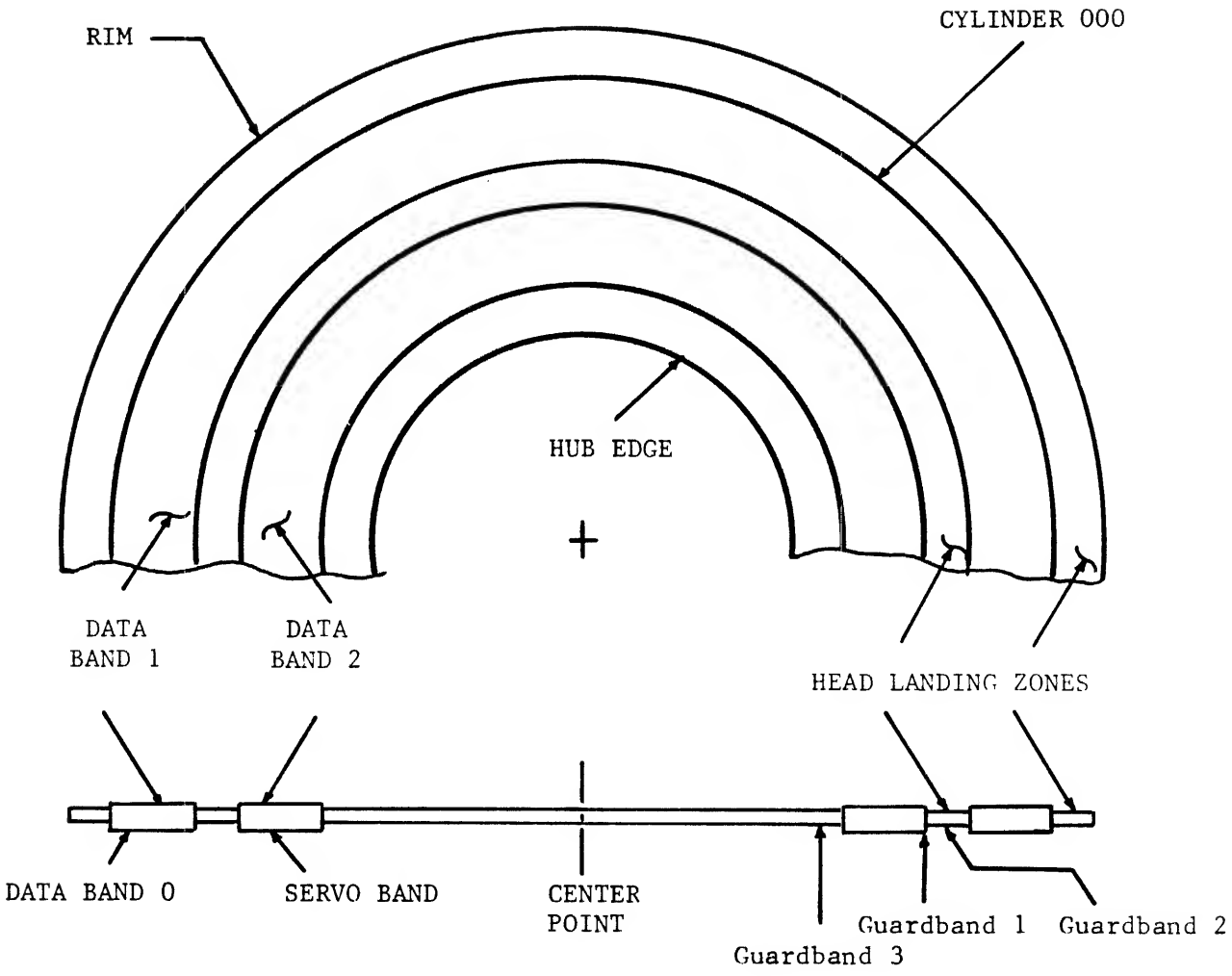



Figure 5.1-1. Servo and Data Surfaces

## 5.3 SERVO PATTERN -- NON-QUADRATURE

A variety of bit patterns are written on the servo tracks to identify the various areas on the servo surface. Figure 5.3-1 shows these patterns. For each pattern illustrated the figure shows the data written on the odd tracks and the even tracks, and the composite signal from the servo read head when it is centered between the two adjacent tracks.

The negative pulses are sync pulses. In the all 0 pattern, these pulses occur at 2-BYTE intervals, and serve to define the bit-cell boundaries. When the servo head reads a 1, an additional negative pulse occurs in the mid-cell position.

The positive pulses are used by the servo circuitry to recognize track crossings or to maintain the on-track condition. Referring again to the all 0 pattern, it can be seen that the positive pulse occurring one-third of the way across the bit-cell is generated by the even track pattern, while the one occurring at the two-thirds point comes from the odd track. The first two patterns are written in the servo data band. The bulk of each track consists of the all 0 (non-index) pattern. The index pattern occurs only once each revolution. It has the same angular position on all servo data tracks, and serves to mark the "0" angular reference point.

The patterns on the three guardbands are repeated at intervals of 512 bytes around the servo track. They serve simply to identify the band in which the servo head is currently located.

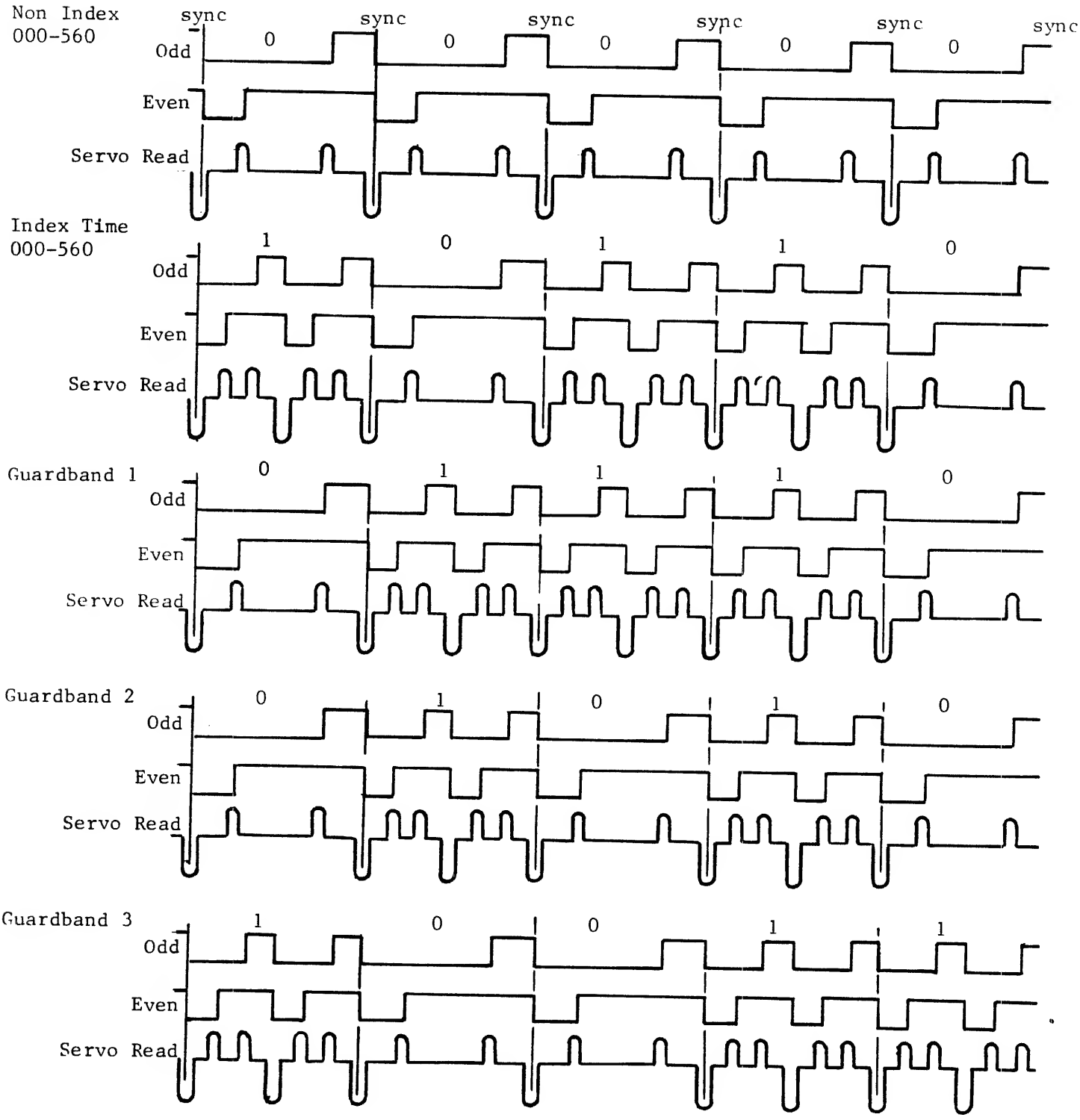



Figure 5.3-1. Servo Track Signals -- Non-Quadrature

## 5.4 SERVO SURFACE -- QUADRATURE

The purpose of the servo surface is to provide a coordinate system by means of which the electrical circuitry of the disc drive can locate specific areas for writing or reading data. The servo surface itself is written once at the factory, and thereafter is a read-only area. The information on the servo surface is used to determine the angular position of the disc, as well as the radial position of the head carriage.

The servo surface is divided into four distinct groups of tracks. From the inside (hub) out, these are as follows:

a. Guardband 3
b. Servo Data Bands
c. Guardband 1
d. Guardband 2 (the Head Landing Zone)

Within each of these bands, there are four types of tracks -- odd normal tracks, odd quadrature tracks, even normal tracks, and even quadrature tracks. Each track type produces a characteristic signal at the servo read head, as described below in the **SERVO PATTERN** section. The closer the servo read head is to a particular track, the greater will be that track's contribution to the servo head's output.

The servo circuitry compares the amplitudes of the signals from adjacent tracks, and identifies an equal-amplitude condition as a "track crossing". During seek operations, the servo circuitry counts the track crossings in order to derive the cylinder address of the data write/read heads. During write and read operations, the servo circuitry adjusts the position of the head carriage in such a manner as to preserve the equal-amplitude condition, thus keeping the write/read head "on track".

## 5.5 SERVO PATTERN -- QUADRATURE

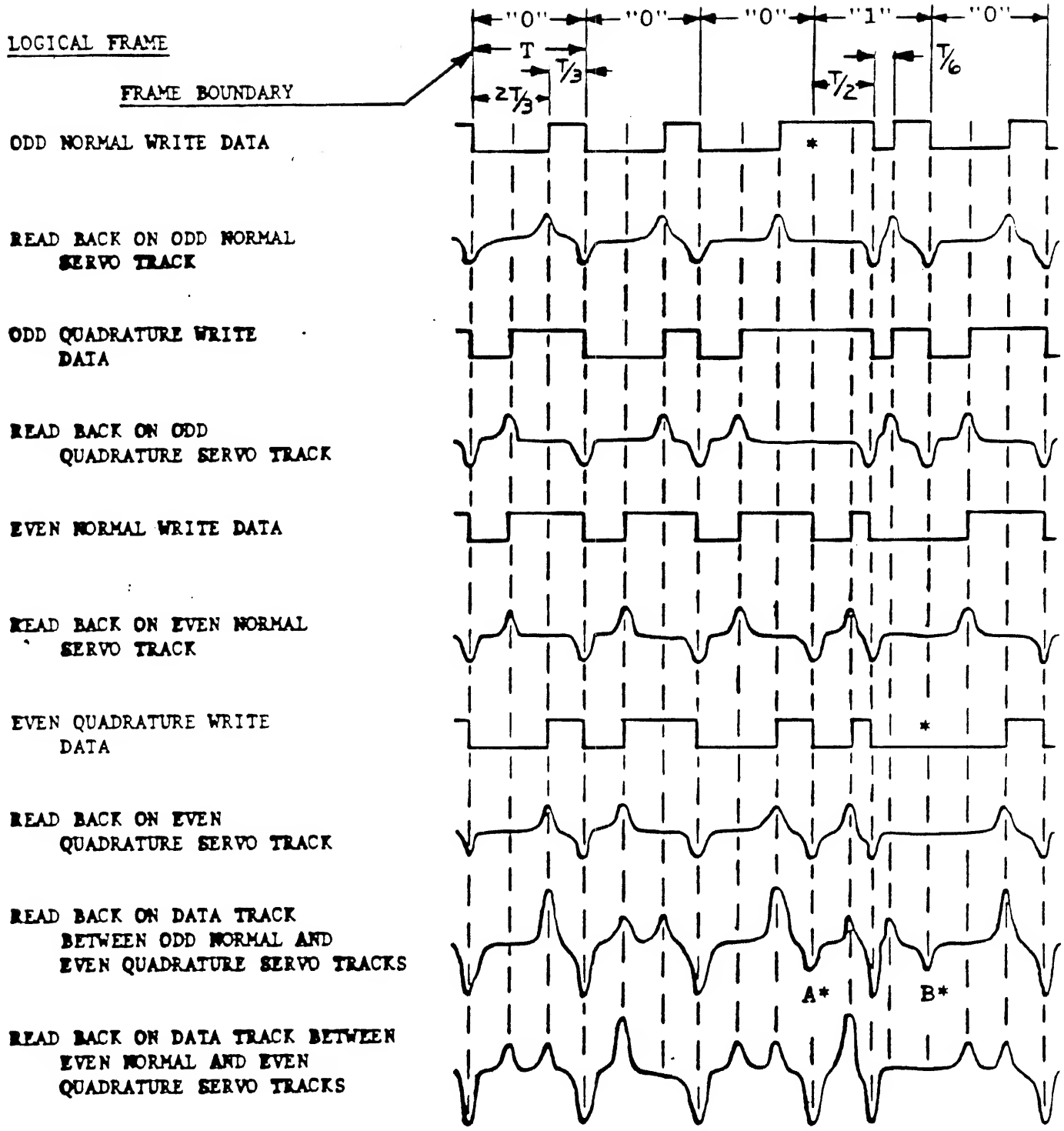
Figure 5.5-1 shows the four kinds of servo track signals. The normal servo data patterns are written on the integer tracks, and the quadrature servo data patterns are written on the half-integer tracks.

The negative pulses are sync pulses. In the all "0" pattern, these pulses occur at regular intervals, and serve to define the frame boundaries. When the servo head reads a "1", an additional negative pulse occurs in the mid-frame position. The frame time interval (T) is equal to 16 write/read data bit times. Most of a given track is written with the "0" pattern. The "1" pattern occurs once each revolution of the disc, and serves to define the INDEX location.

The positive pulses are used by the servo circuitry to recognize track crossings or to maintain the on-track condition. Referring again to the all "0" pattern, it can be seen that the even normal track generates positive pulses occurring one-third of the way across the frame, while the odd normal track generates positive pulses occurring at the two-thirds point. The quadrature track patterns have positive pulses alternately at the one-third and two-thirds positions.

When the servo read head is midway between two adjacent tracks (a "track-crossing" position) the output resembles the patterns shown at the bottom of Figure 5.5-1. Successive frames produce the equal-amplitude positive peaks, alternating with single large peaks. By analysing which frames have the equal-amplitude peaks, and whether the large peaks occur at the one-third or the two-thirds locations within the frame, the servo circuitry is able to determine which of the four kinds of "track-crossing" positions is being indicated. Note that the servo read head is midway between two adjacent tracks when the data write/read heads are "on-track".

The servo circuitry counts the track crossings in order to determine the current cylinder address. In the 3350, data tracks are written at alternate cylinder address (all integer or all half-interger). In the 6650 and 15450, data tracks are written at both integer and half-integer cylinder addresses.




* Missing sync at the frame boundary will result in low amplitude signal as shown at A* and B*

Figure 5.5-1. Servo Track Signals -- Quadrature

## 5.6 DATA SURFACE

The configuration of tracks on the data surfaces has a one-to-one correspondence with the configuration of servo tracks on the servo surface. Thus, for example, when the servo head is in the servo data band, all the write/read heads are in the corresponding positions in their respective write/read data bands. When the servo head is in the servo landing zone, each data head is also in its own landing zone.

The write/read data tracks are numbered consecutively, starting with track 0 nearest the outside edge of the disc. Each write/read data track is divided into sectors. The division of tracks into sectors can be adjusted by the user through switch settings on the main PCB, as detailed in the **INSTALLATION** section.

## 5.7 SECTOR FORMAT

In a typical sector format, each track is divided as follows:

Index Mark

Gap (type 1)

Skip Defect Record

N identical Data Sectors

Gap (type 3)

The index mark is a 1.92 microsecond (two-byte times) pulse, derived from the index pattern on the servo data surface.

The type 1 gap allows for VFO synchronization for data separation. It consists of zeros, and has a minimum length of 23 bytes.

The composition of the Skip Defect Record and of the N identical Data Sectors are described below.

The type 3 gap is a function of sector size, and is used to fill (with zeros) the space left over after the largest possible integer number of sectors (commensurate with the switch settings) have been written.

It should always be remembered that the switch settings (determining sector size) are read by the microprocessor as part of the Sequence Up process. Thus, a change in these switch settings will not take effect until the drive is once again sequenced up, or re-initialized from a power down condition.

The Skip Defect Record can identify up to three defective sectors on the track. The format for the Skip Defect Record is as follows:

| | |
|---|---|
| Data sync (FB hex) | 1 byte |
| 1st defect address | 2 bytes |
| 2nd defect address | 2 bytes |
| 3rd defect address | 2 bytes |
| Check sum | 2 bytes |
| Fill characters (zeros) | 2 bytes |

The N identical Data Sectors have the following structure:

Sector Mark
Gap (type 1) -- zeros (23 bytes minimum)
Address Field
Gap (type 2) -- zeros (11 bytes minimum)
Data Field

The sector mark is a 960 nanosecond (one byte time) pulse which occurs at the beginning of each sector. It is generated by the servo circuitry, using a byte clock which is initialized by the index pulse.

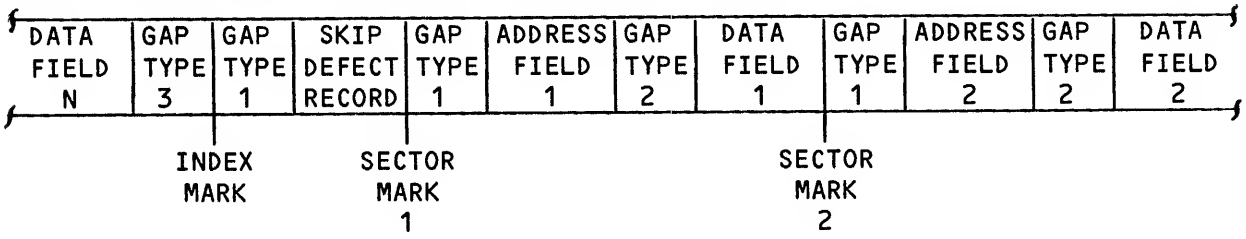
The format for the Address Field is as follows:

| | |
|---|---|
| Sync pattern (F9 hex) | 1 byte |
| Head and high order cylinder address | 1 byte |
| Low order cylinder address | 1 byte |
| Sector address | 1 byte |
| Sector length and flag | 1 byte |
| CRC | 2 bytes |
| Fill characters (zeros) | 2 bytes |

The Data Field has the following structure:

| | |
|---|---|
| Sync pattern (FD hex) | 1 byte |
| Data bytes (according to sector length) | |
| CRC | 2 bytes |
| Fill characters (zeros) | 2 bytes |

The following diagram summarizes the sector format:



# SECTION 6 - ELECTRICAL CIRCUIT OPERATION

## 6.1 OVERVIEW

Figure 6.1-1 is a simplified block diagram of the PRIAM 3350 disc drive with the standard PRIAM interface. The overall organization shown is the same for all drives in the 14" family. The 15450, however, has two magnetic discs and seven data heads, rather than the single disc and three data heads. Also the names of the specific interface signals vary as a function of the interface option present.

With the exception of the head disc assembly and the motor control assembly, everything shown in Figure 6.1-1 is located on the main PCB. The disc drive has its own (8035) microprocessor, which controls the sequencing of all the operations that occur in the drive. Detailed flowcharts showing these operations step-by-step are given below in the **MICROPROCESSOR FLOW CHARTS** section.

## 6.2 DRIVE SELECTION

The disc drive must be properly selected before it will respond to any of the signals on the controller interface. On the standard PRIAM interface, this is accomplished by placing the proper address on the DRIVE SELECT 1-4 lines. On the SMD interface, the UNIT SELECT TAG line is activated, and the proper address is placed on the UNIT SELECT 1, 2, 4, and 8 lines. In general, the interface lines to be used may be determined by referring to the section (below) describing the specific interface involved.

The address of an individual drive is determined by switch settings on the main PCB, as discussed in the **INSTALLATION** section. The drive responds to the selection procedure only when its switch-selected address matches that placed on the interface by the controller.

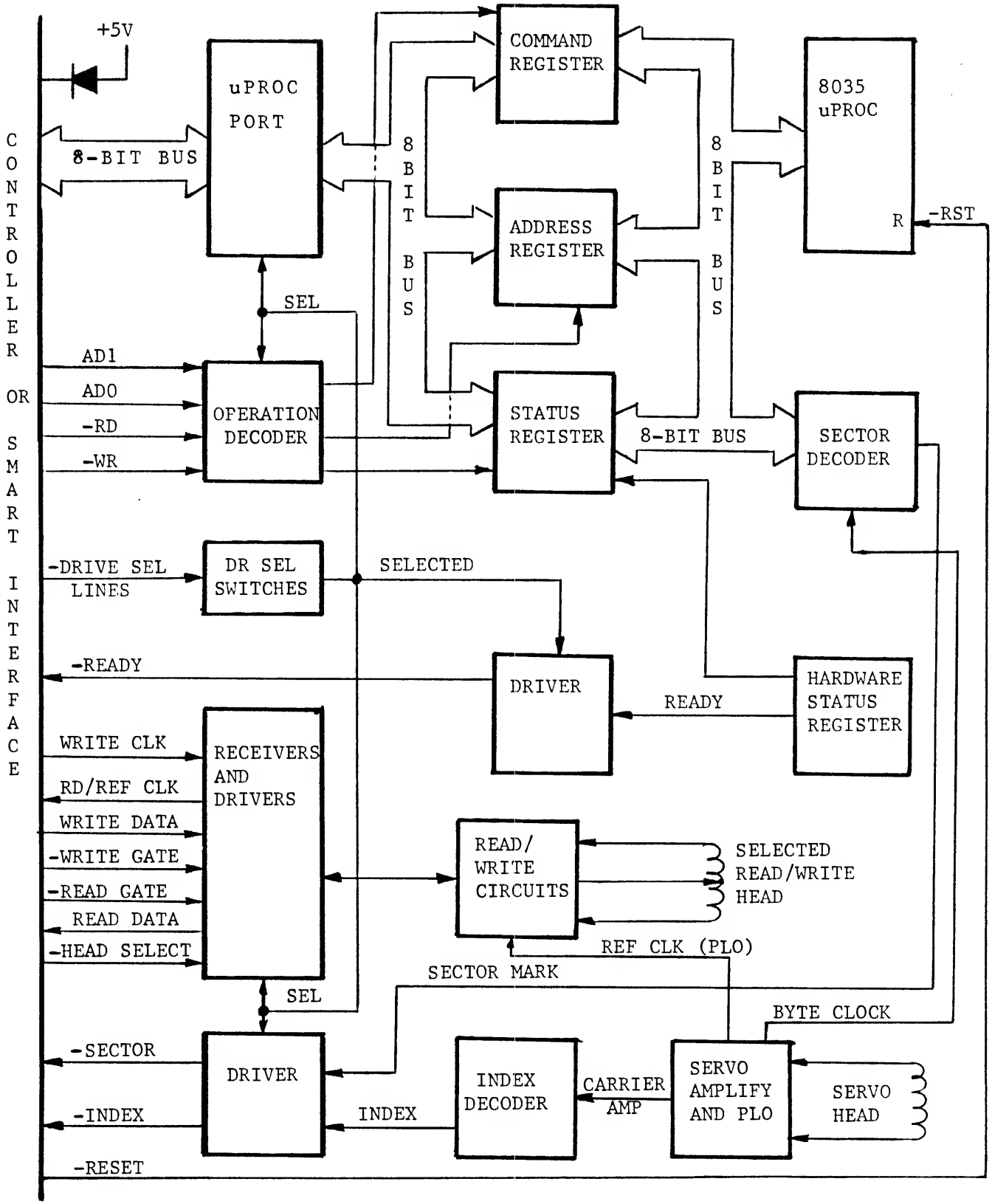



Figure 6.1-1. Simplified Block Diagram of a PRIAM 14-inch Disc Drive

## 6.3 POWER UP/DOWN SEQUENCES

When power is applied to the main PCB, the Microprocessor Initialization sequence occurs automatically. The microprocessor then goes into the idle state, in which it monitors the controller interface for a command. See the INIT and IDLE flow charts for details.

The controller may then issue a Sequence Up command to the drive (the exact manner in which this is done depends on the interface option present). The microprocessor recognizes this command and starts the spindle motor. When the motor is running at the proper speed, the microprocessor reads the sector length switches, and configures the drive to operate in terms of the chosen sector length. Next it calls the RSTRGO subroutine, which moves the heads to CYLINDER ZERO.

It then enables the drive ready status, resets the busy condition, and returns to the idle state. See the CMDET, SEQUP, RSTRGO, and CMDEND flow charts for details.

The drive is stopped by issuing a Sequence Down command. This causes the heads to return to the landing zone, and stops the spindle motor. See the SEQDWN and RSTR1 flow charts for details.

## 6.4 MOTOR CONTROL CIRCUITRY

The spindle motor is a brushless (electronic commutating) permanent magnet DC motor. The speed of the motor is controlled by a closed-loop circuit containing an optical position encoder and a comparator. In drives shipped after October 1980 a crystal comparator is used.

The position of the rotor relative to the stator is encoded. Two $90^{o}$ shutters are attached to the spindle motor rotor and three phototransistors (mounted $30^{o}$ apart) are attached to the photocell circuit board. Each phototransistor stops conducting when a shutter blocks its infrared LED light source.

With the exception of the phototransistors and the spindle motor itself, all spindle rotation circuitry is located in the motor control assembly.

Figure 6.4-1 is a block diagram of the motor control circuitry. At the point marked J2-4 the microprocessor sets the OFF signal true to inhibit spindle rotation, or false to allow spindle rotation. The microprocessor monitors the speed of spindle rotation. If, during the power up sequence, the motor does not reach its specified speed within one minute, or if, during normal operation, the motor speed passes outside the specified speed range, the microprocessor will set the Fault condition, restore the heads to the landing zone, and inhibit the spindle rotation.

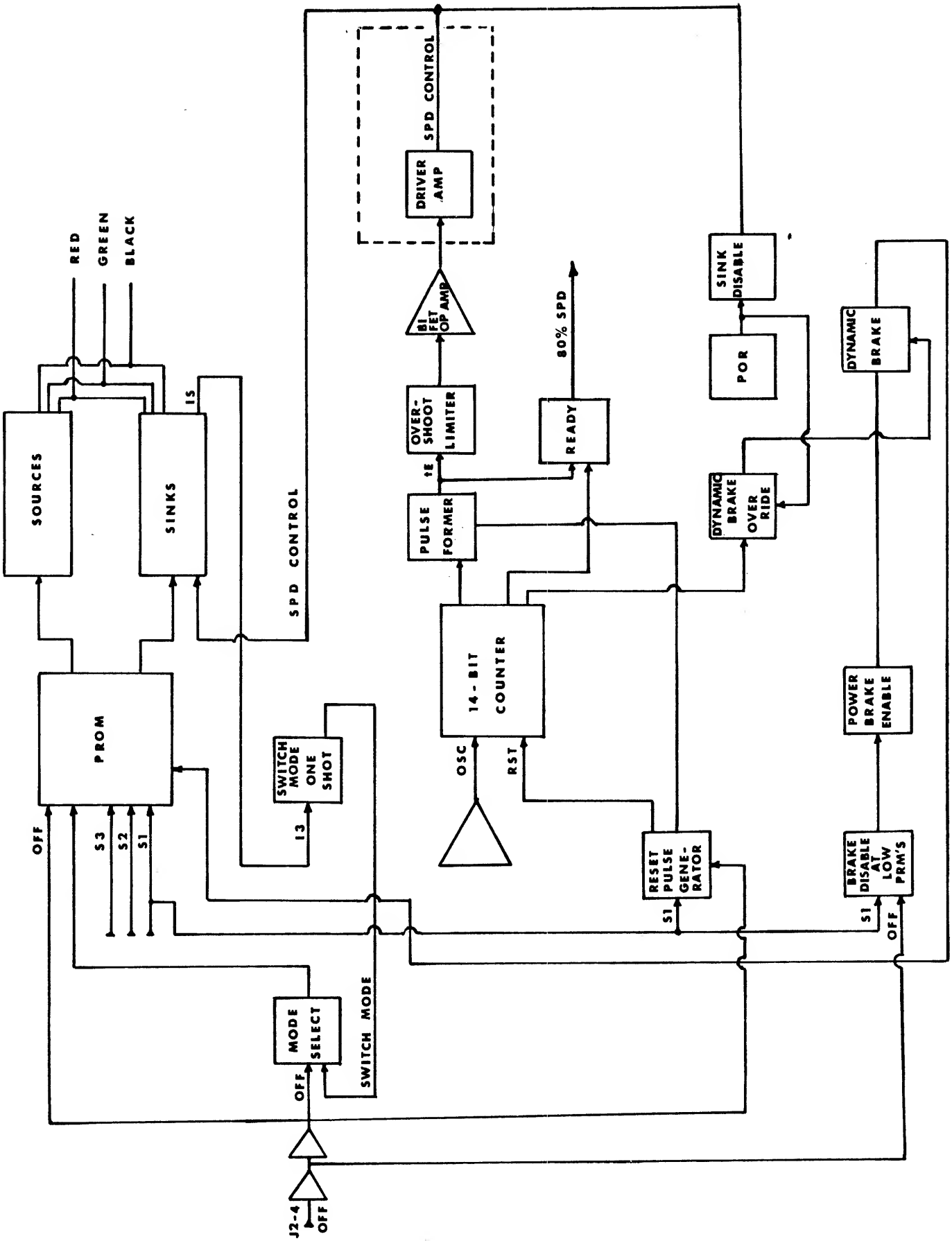



Figure 6.4-1. Motor Controller

## 6.5 SEEK MODES

The servo system has two main modes of operation -- On Track mode (also called Position mode) and Move mode.

Move mode becomes active when the drive is commanded to move the heads. The microprocessor receives the new target cylinder address and the seek command, determines the direction of travel and the number of tracks to be crossed, and sets Move mode.

When the servo is in Move mode, a velocity profile (produced by a digital-to-analog converter) is compared (via a summing junction) with the output of an electronic tachometer, which indicates the velocity of head motion. The difference signal from the summing junction is fed to the servo power amplifiers, which control the voice coil motion. The heads are driven toward the new cylinder address. The servo circuitry monitors the track crossings and decreases the velocity of head motion as the selected cylinder is approached.

When the heads are within 100 microinches of the new cylinder, the On Track mode becomes active.

In the On Track mode, the heads are held precisely over the designated track. Any unintended head movement is detected by the electronic tachometer and fed to the summing junction. This in turn causes the servo power amplifiers to adjust the head position, so that the heads remain at the desired location.

Servo safety circuits drive the heads to the landing zone upon detection of a low power condition, or if both Move and On Track modes occur simultaneously. The safety circuits also monitor the voice coil speed. If the specified speed is exceeded, or if the continuous position information is lost, an Overspeed signal is established and the servo power amplifiers are disabled. Seek Fault is set if any of the above conditions develop.

For more details, refer to the SEEK, SEEKGO, LAND, HTRK, TRXING, SKDNE, SKCMP, and SKERR flow charts.

## 6.6 SERVO CIRCUITRY

Figure 6.6-1 is a block diagram of the head carriage servo circuitry. The signal from the servo head is amplified by a preamp located adjacent to the head in the head disc assembly. On the main PCB it is further amplified by an AGC amplifier. The output of this amplifier has the waveform shown as ABCD in the figure, when the servo head is located midway between an odd track and an even track, and the servo data pattern is all 0s. A and D are the sync pulses occurring at the bit cell boundaries. When a 1 is present in the servo data stream, an additional "sync" pulse appears at the mid-cell position.

A sync detect circuit detects the sync pulses at the A and D positions, and uses these pulses as input for the PLO (phase locked oscillator), which generates a steady clock signal of approximately 16 MHz, which is phased locked to the servo data.

The 1s and 0s in the bit stream are identified and sent through a 5-bit shift register. The bit configuration in the shift register is monitored by a decoder, which recognizes the bit patterns that correspond to the index pattern, and to the three guardband patterns.

The pulses marked C and B are the pulses that occur at the 1/3 and 2/3 points in the bit cell. The pattern shown in Figure 6.6-1 corresponds to an all 0s servo data stream. The pulse at point B is the contribution from the even servo track, while the pulse at point C comes from the odd track.

In the On Track mode, the Position Demodulator and On Track Compensator are use to compare the B and C amplitudes, and to apply any discrepancies as an error signal to the input of the voice coil power amplifier, in such a way that the servo head remains midway between the two tracks.

In the Move mode, the B and C amplitudes are monitored, and the threshold detector identifies the track crossings, outputting a TRK XING signal which is used to update a cylinder address counter. The Velocity Tachometer, Curve Generator, and Integrator Combiner together control the input to the voice coil power amplifier, in order to control the head carriage velocity.

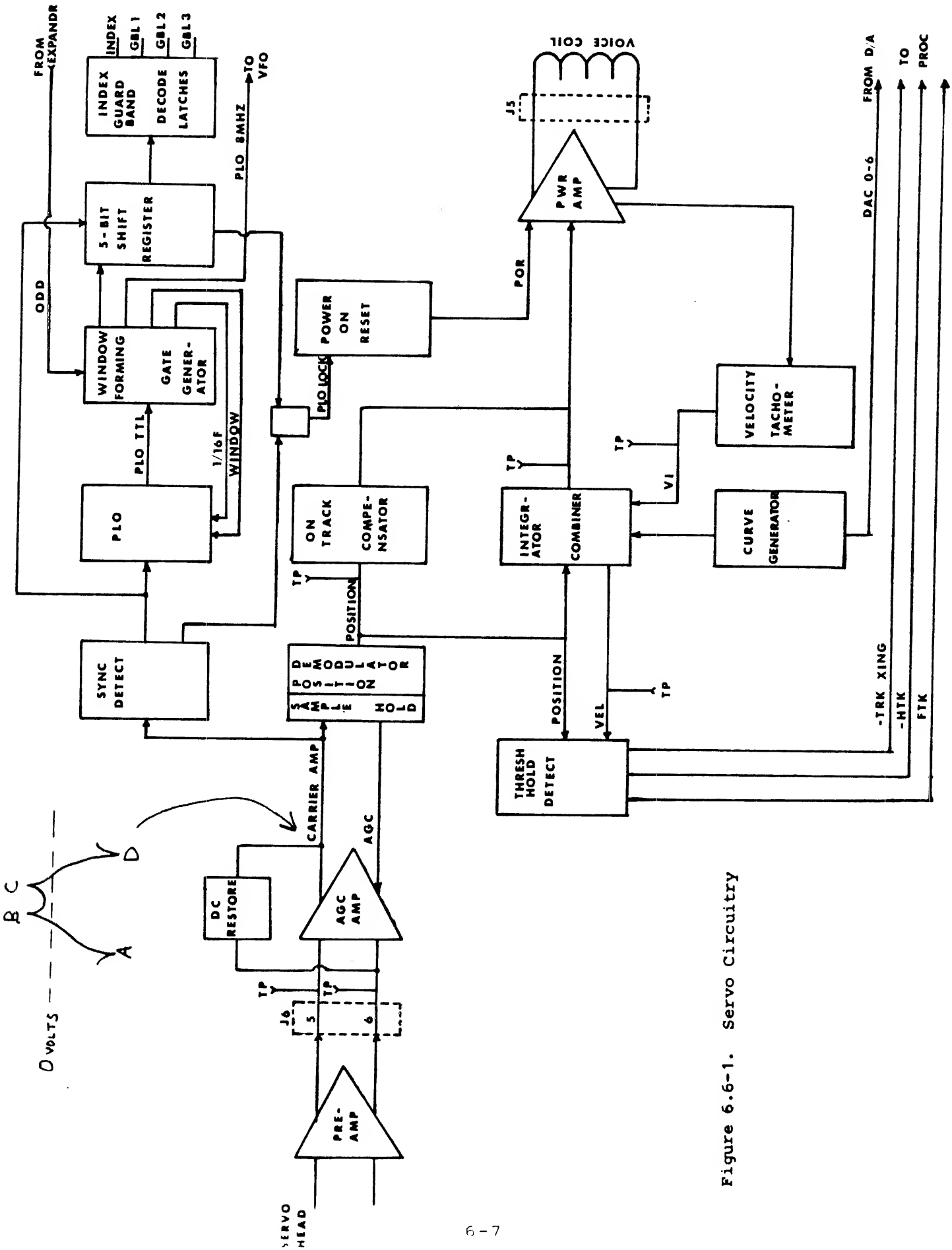



Figure 6.6-1. Servo Circuitry

## 6.7 DATA READ/WRITE FUNCTIONS

PRIAM disc drives use the MFM (modified frequency modulation) recording method. The MFM coding rules determine the relationship between the flux transitions on the recording medium, the data being written, and the bit cell boundaries. The following three rules must be observed:

If a 1 is written, there is a flux transition at the center of the bit cell.

There is always a flux transition at the bit cell boundary between consecutive 0s.

There is never a flux transition at the boundary of a 0 and a 1.

Figure 6.7-1 shows how the MFM encoding works out in practice. The bit cells are 120 nanoseconds long, which corresponds to a data read/write rate of approximately 8 megabits per second. The MFM technique assures that there will never be more than two bit-cell times between successive flux transitions, and thus there will always be enough information to properly reconstruct and synchronize the original NRZ data.

As shown in Figure 6.7-1, the write current to the selected data head changes direction at each of the MFM transition points. The magnetization on the disc is proportional to this current. During read operations, the signal from the read head is as shown on the ANALOG MFM line. The signal is then differentiated, zero crossings are detected, and these (adjusted to the nearby bit-cell boundary or mid point) become the transitions of the LIMITED DATA line, which matches the original MFM data. A data separator later converts this back into NRZ data.

Figure 6.7-2 is a block diagram of the circuitry involved in the write operation. The controller initiates a write operation by supplying the disc drive with Head Select, Write Gate, Write Clock, and NRZ Write Data. If the drive is selected and ready and if Write Protect is off, the write operation will begin. The write circuits will encode the NRZ data to MFM, synchronize the data to the write clock, and record the data transitions on the selected disc surface.

Safety circuits monitor the write operation. If a fault is detected, writing is inhibited, Fault is set, and Ready is inhibited.

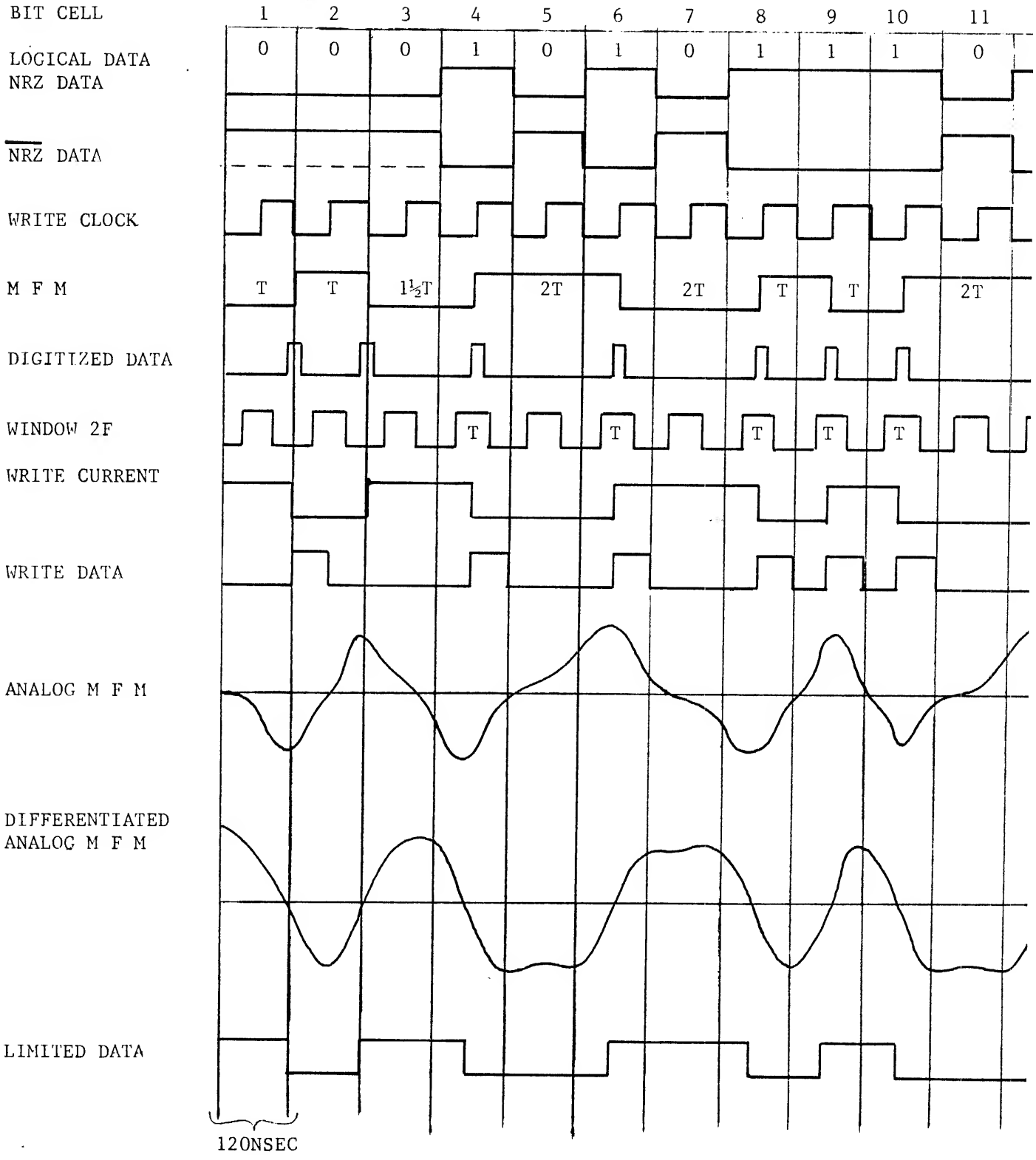



Figure 6.7-1. Read/Write Timing and Encoding

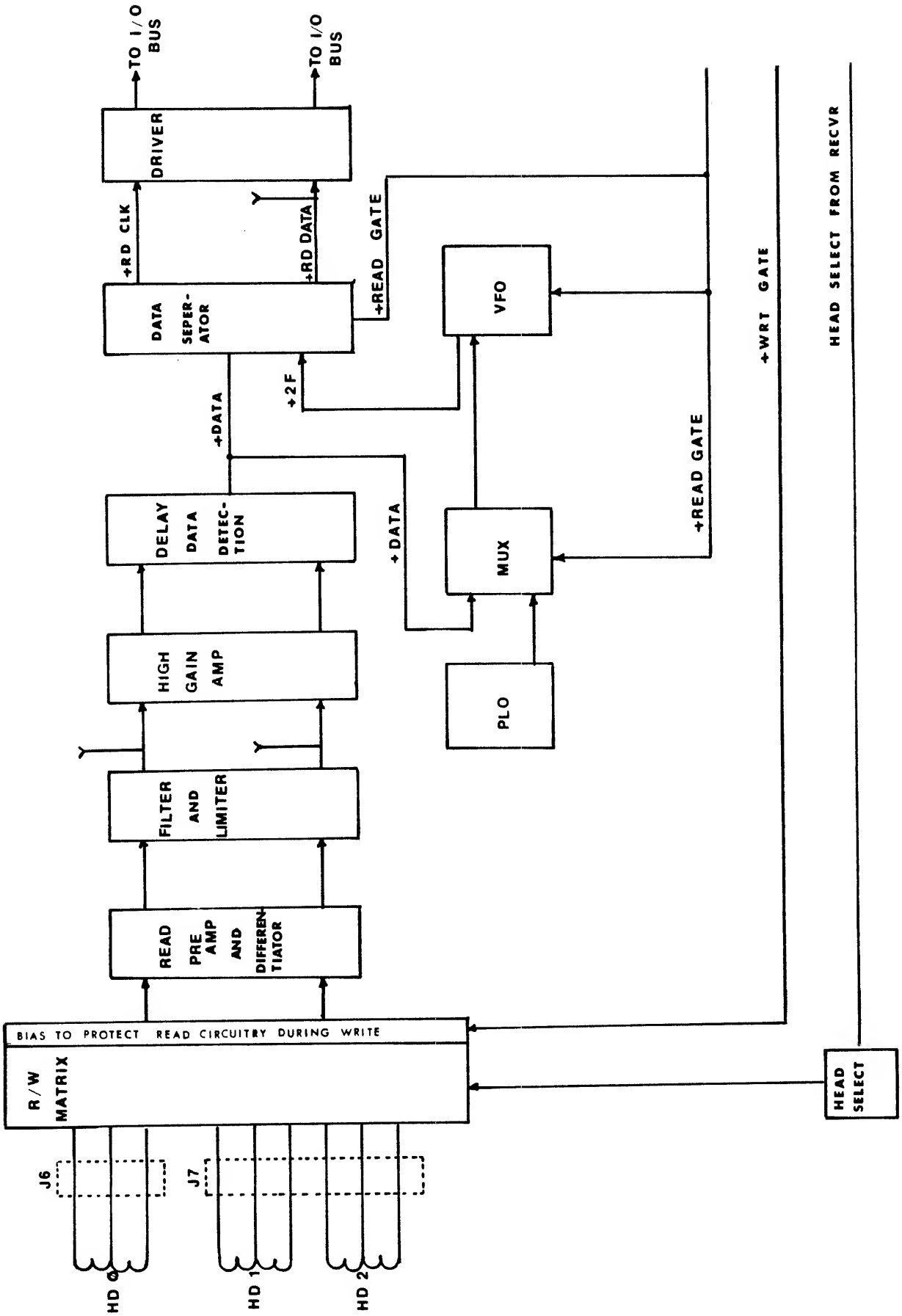



Figure 6.7-2. Data Write Circuitry

Figure 6.7-3 is a block diagram of the circuitry involved in the read operation. The controller initiates a read operation by supplying the disc drive with Head Select and Read Gate. The controller sets Read Gate true in the gap area immediately preceding the desired data. The gap area serves to allow time for the data separation circuits to synchronize to the recorded data.

During the read operation, voltage peaks of alternate polarities are induced in the selected head. A voltage peak occurs at each detected data transition. The following functions are performed by the read circuitry:

1. Amplify, differentiate, and digitize the signal from the read head.
2. Verify the pulse width of the digital data and eliminate any false zero crossings.
3. Separate the data pulses from the clock pulses.
4. Discard the detected clock pulses.
5. Transform the data pulses to the NRZ format.
6. Develop a Read Clock signal to identify the beginning of each bit cell.
7. Transmit the NRZ data and Read Clock to the controller.

A recoverable read error (soft error) resulting from a transient condition can usually be corrected by re-reading the particular record involved. An error of this type is normally detected by the cyclic redundancy checking (CRC) performed by the controller.

A non-recoverable error (hard error) is one which persists after several attempts to read the record. This may be a write error, in which case the error is cleared by re-writing the record. A hard error may also be caused by a disc surface defect, in which case the error may persist even after the record has been re-written.

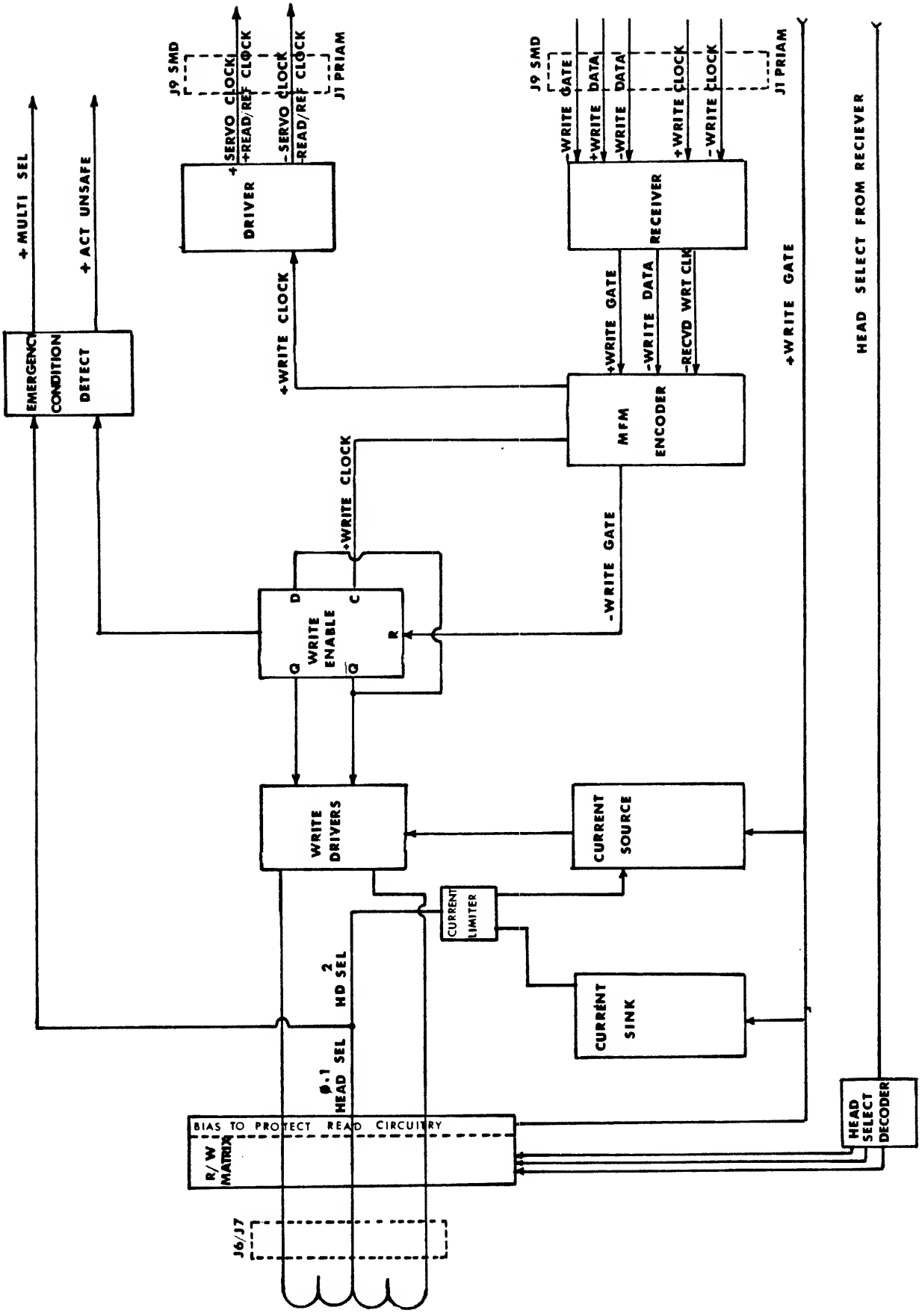



Figure 6.7-3. Data Read Circuitry

## 6.8 PLO/VFO

Two of the circuits shown in Figure 6.7-3 are used to provide the proper synchronization between the information recorded on the disc and the data being transferred over the interface to the controller. The PLO proceeds at a uniform rate, while the VFO is subject to variations because of the analog nature of the write and read operations at the disc and head level.

The VFO generates the clock signals to be sent to the controller. During data read operations the raw data stream is used as a source of sync signals. The VFO adjusts its output clock frequency in such a manner that the bit rate at the interface is equal to the average rate at which the bit cell boundaries are detected in the raw data stream.

During procedures other than read operations, there is no data stream to synchronize to. At these times the input to the VFO comes from the PLO, which operates continuously from the servo data. Thus, for example, during write operations, the PLO generates a surrogate clock to which the VFO becomes a slave. The VFO output is used to generate the Read Clock signal to the controller. The controller then uses this signal as a basis for the Write Clock signal it returns with the data to be written.

## 6.9 MICROPROCESSOR FLOW CHARTS

This section contains the flow charts that gives details on the microprocessor controlled sequences used in the disc drive. When power is initially applied to the main PCB, the INIT routine is automatically executed. The microprocessor then enters the IDLE state, where it waits for a command, as shown in the IDLE flow chart.

If a command is received, the CMDET routine is executed. If the command is not rejected (CMDREJ) the microprocessor executes the particular command routine specified.

Power sequencing for the spindle motor is controlled by the SEQUP and SEQDWN routines. Seek operations are controlled by the RESTOR and SEEK routines, and their subroutines RSTR1, RSTRGO, SEEKGO, LAND, HTRK, TRXING. Seek operations terminate with the SKDNE, SKCMP, or SKERR routines. Commands in general terminate with the CMDEND or CMDREJ routines.

The Fault Reset command is executed by the FLTRST routine.

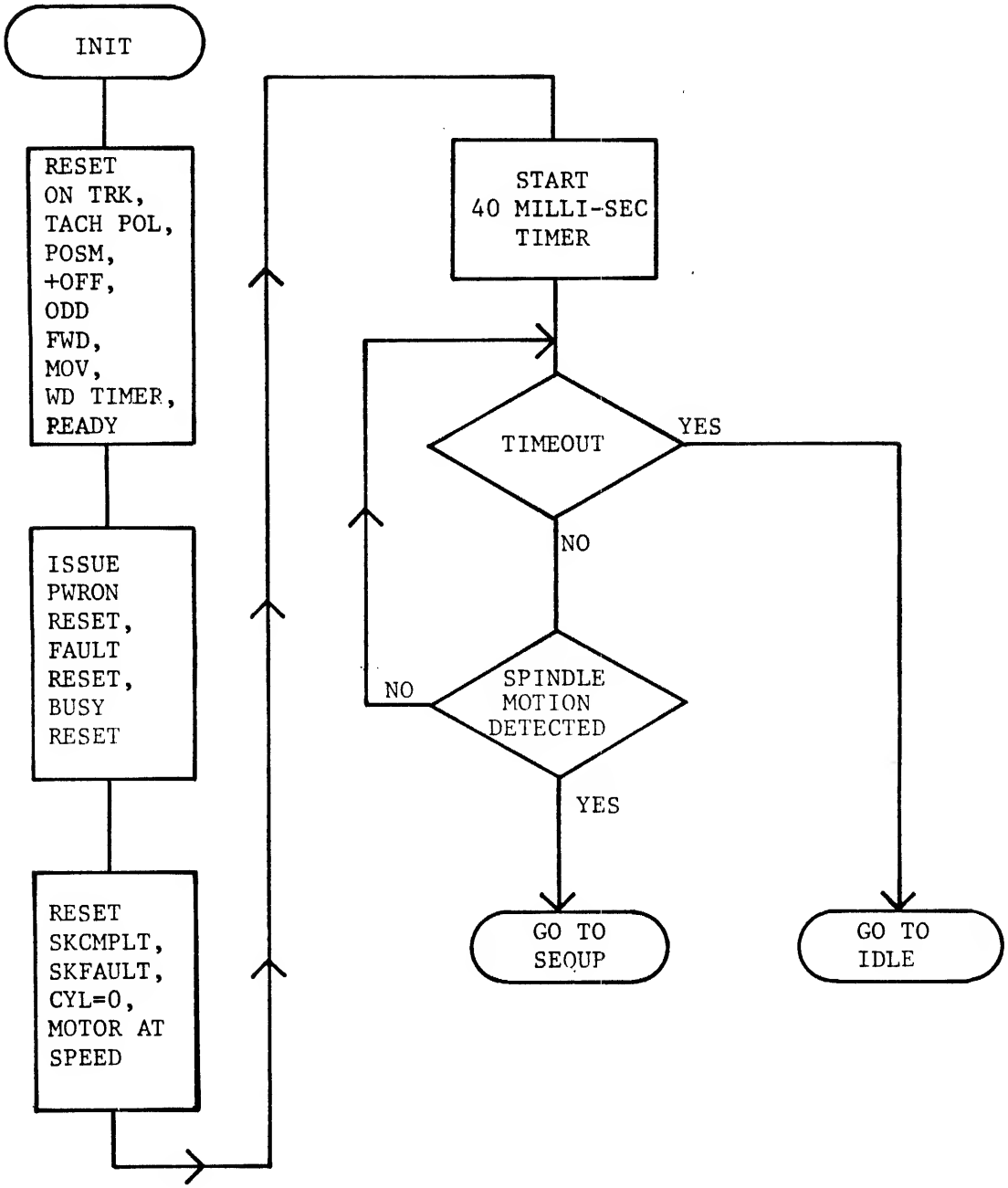



Figure 6.9-1. Initialization Flow Chart

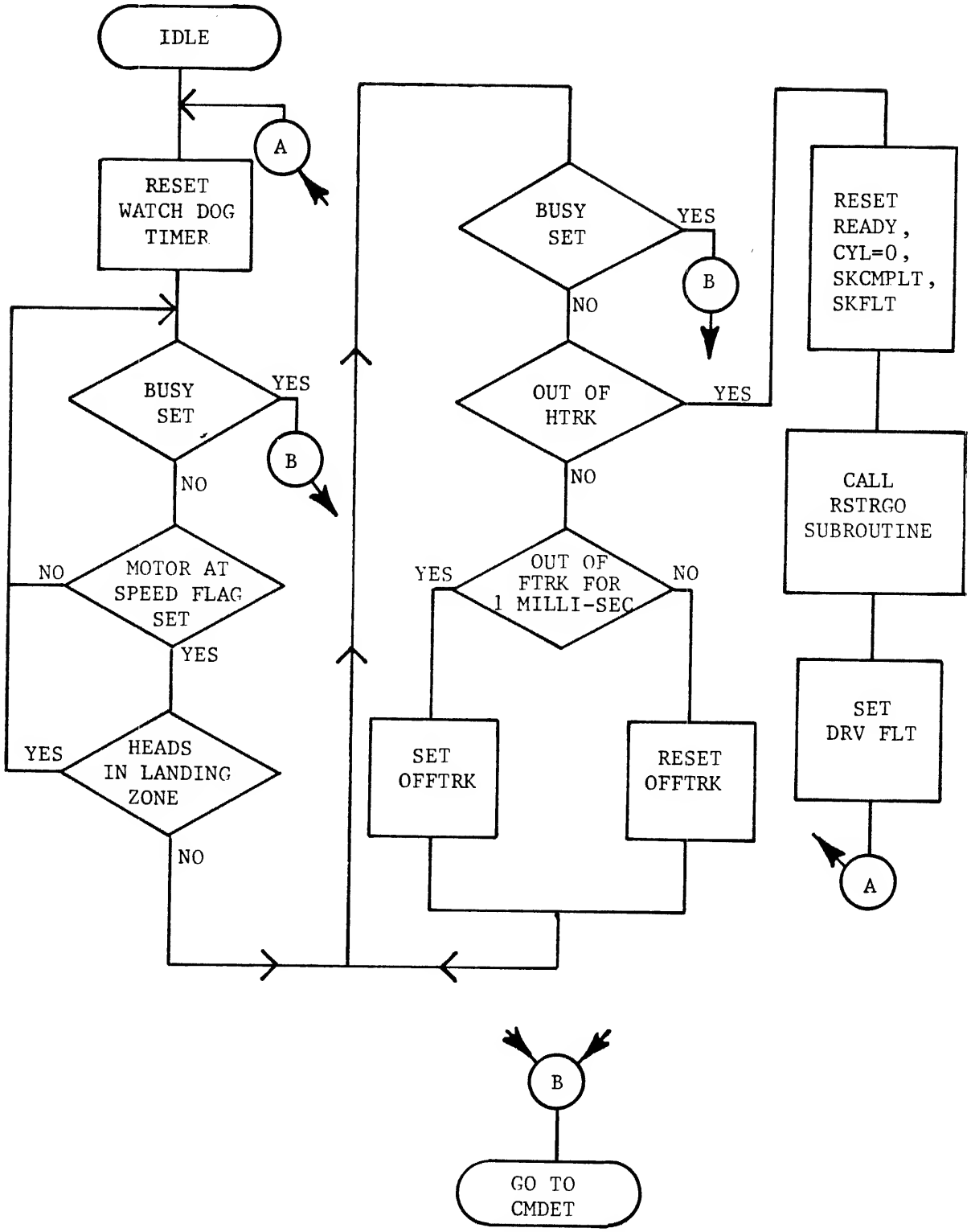



Figure 6.9-2. Idle Flow Chart

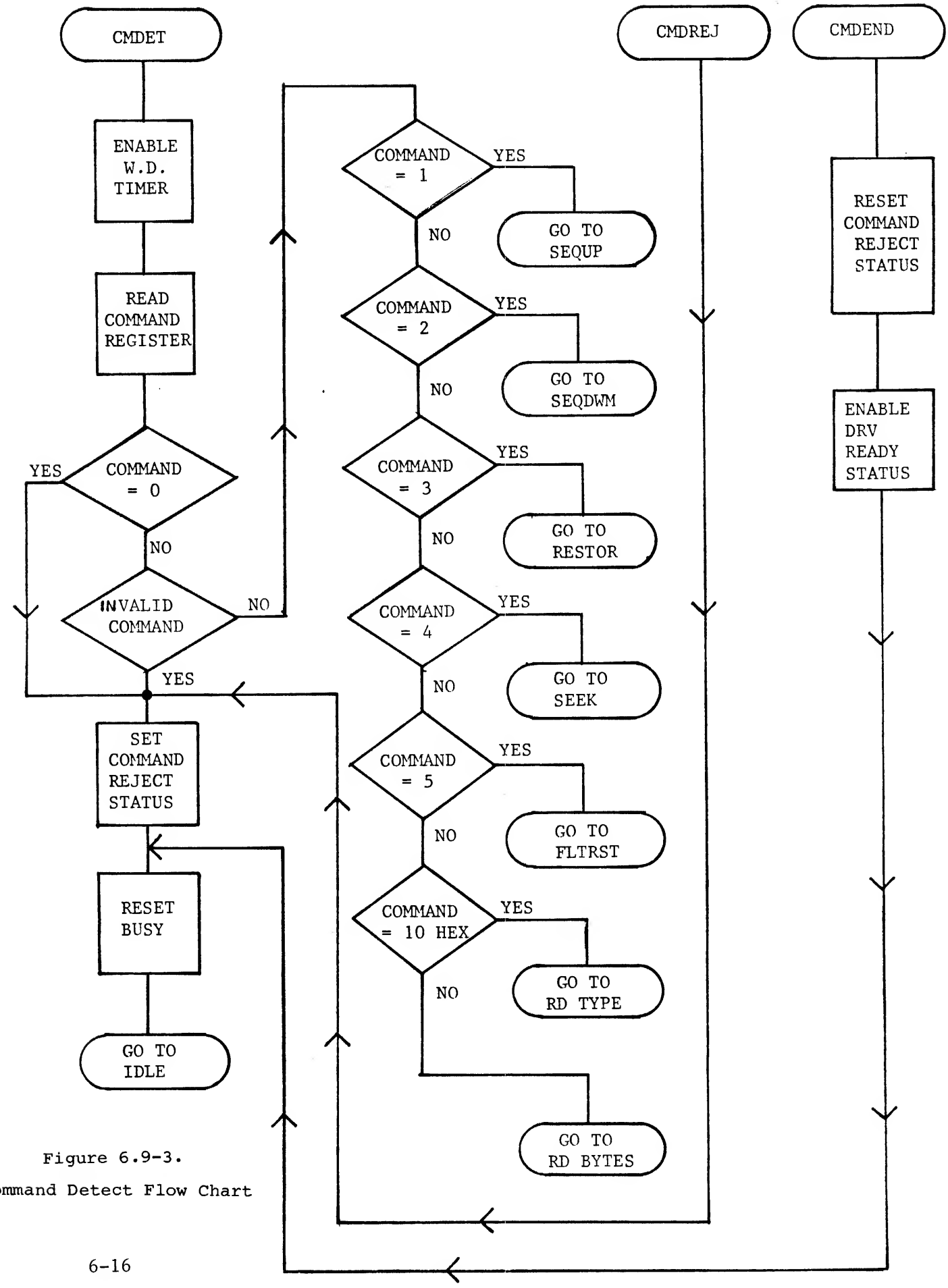



Figure 6.9-3.

Command Detect Flow Chart

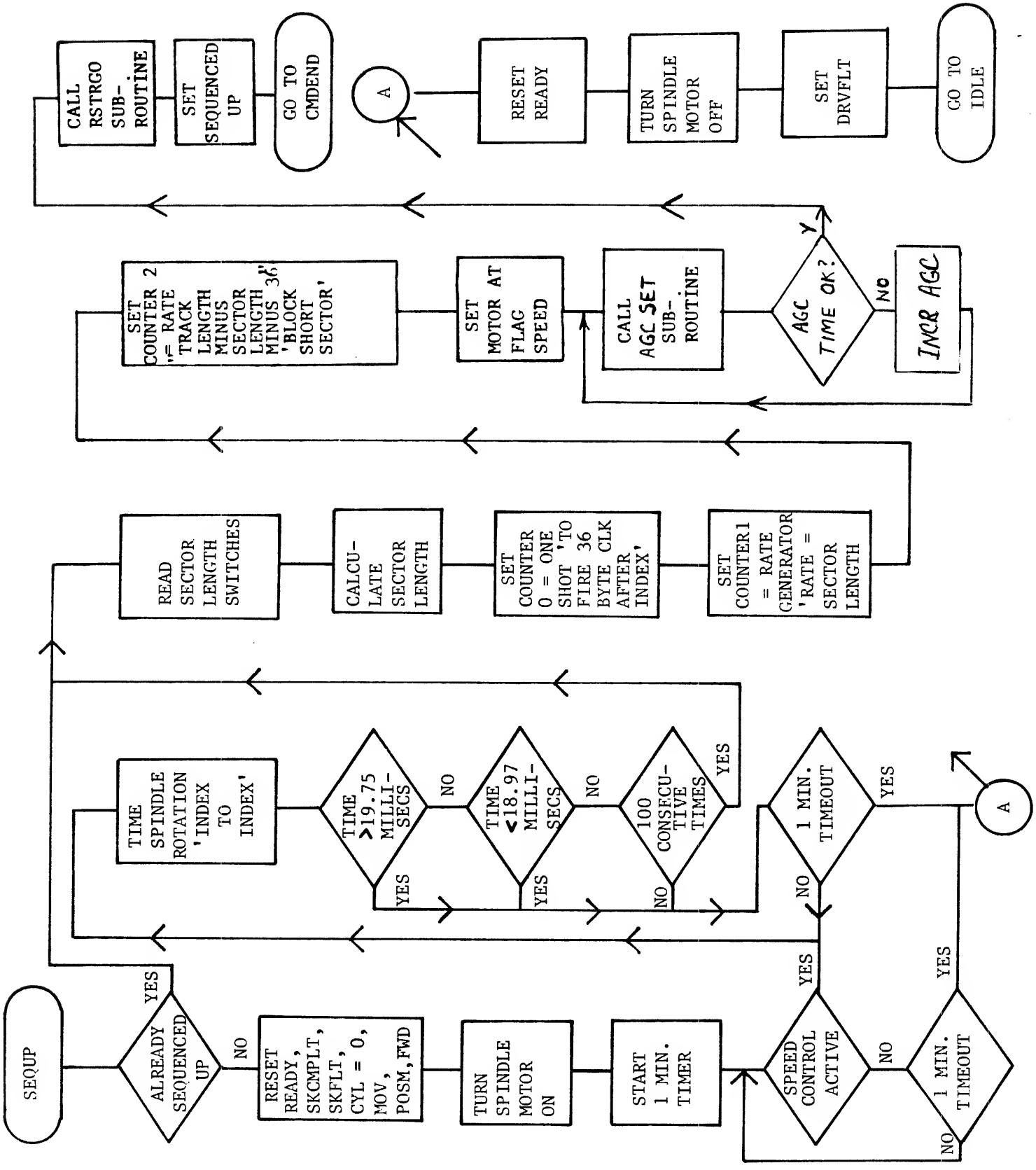



Figure 6.9-4. Sequence Up Flow Chart

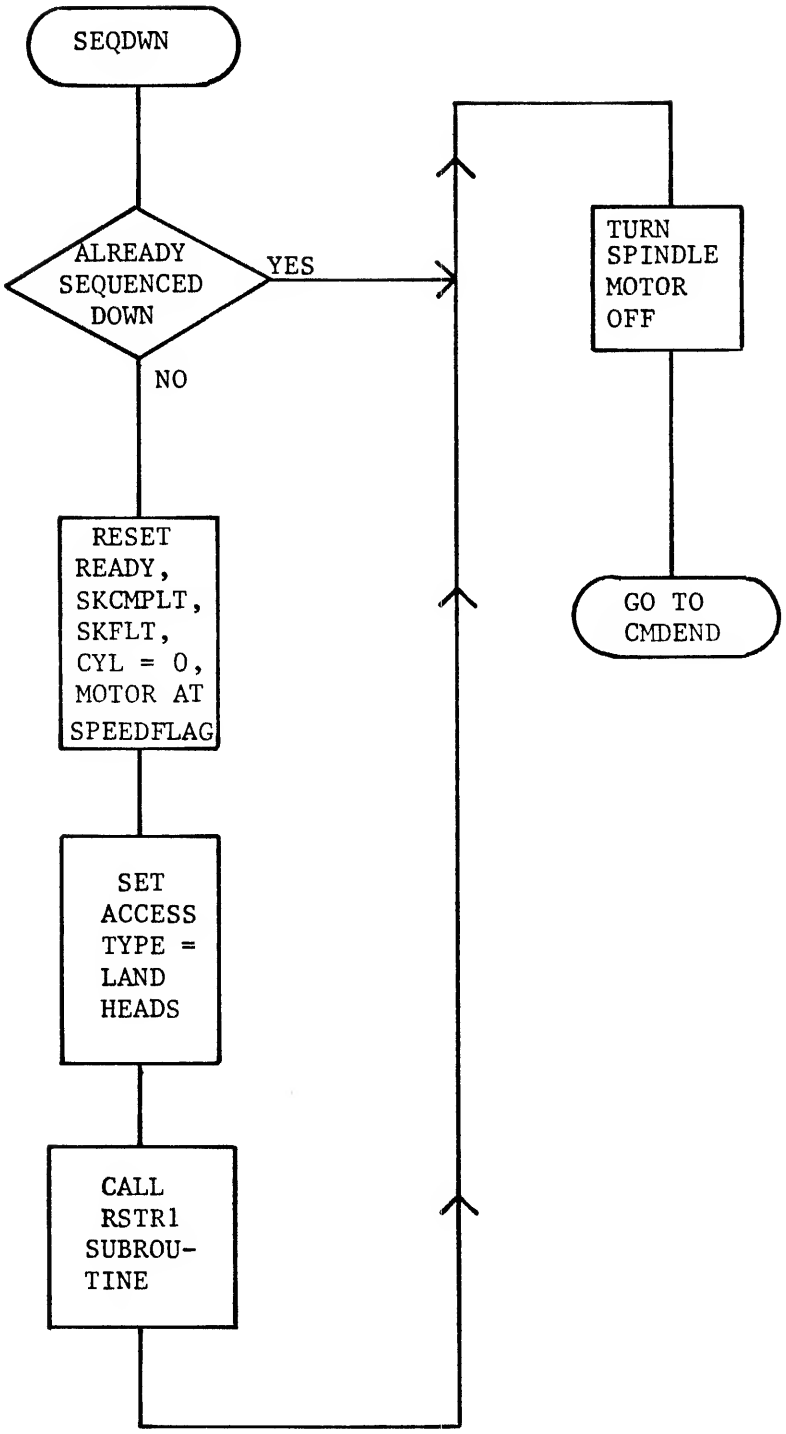



Figure 6.9-5. Sequence Down Flow Chart

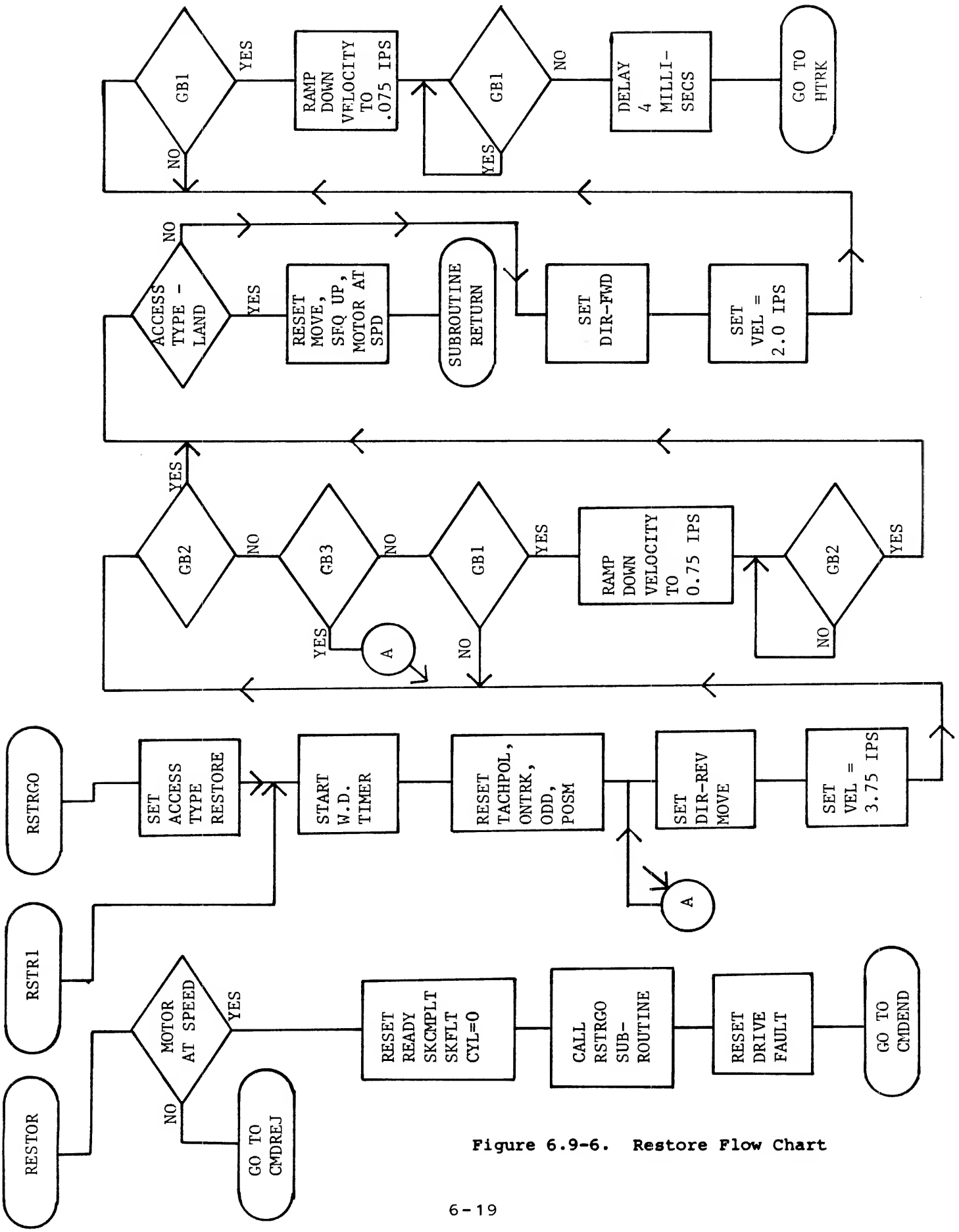



**Figure 6.9-6. Restore Flow Chart**

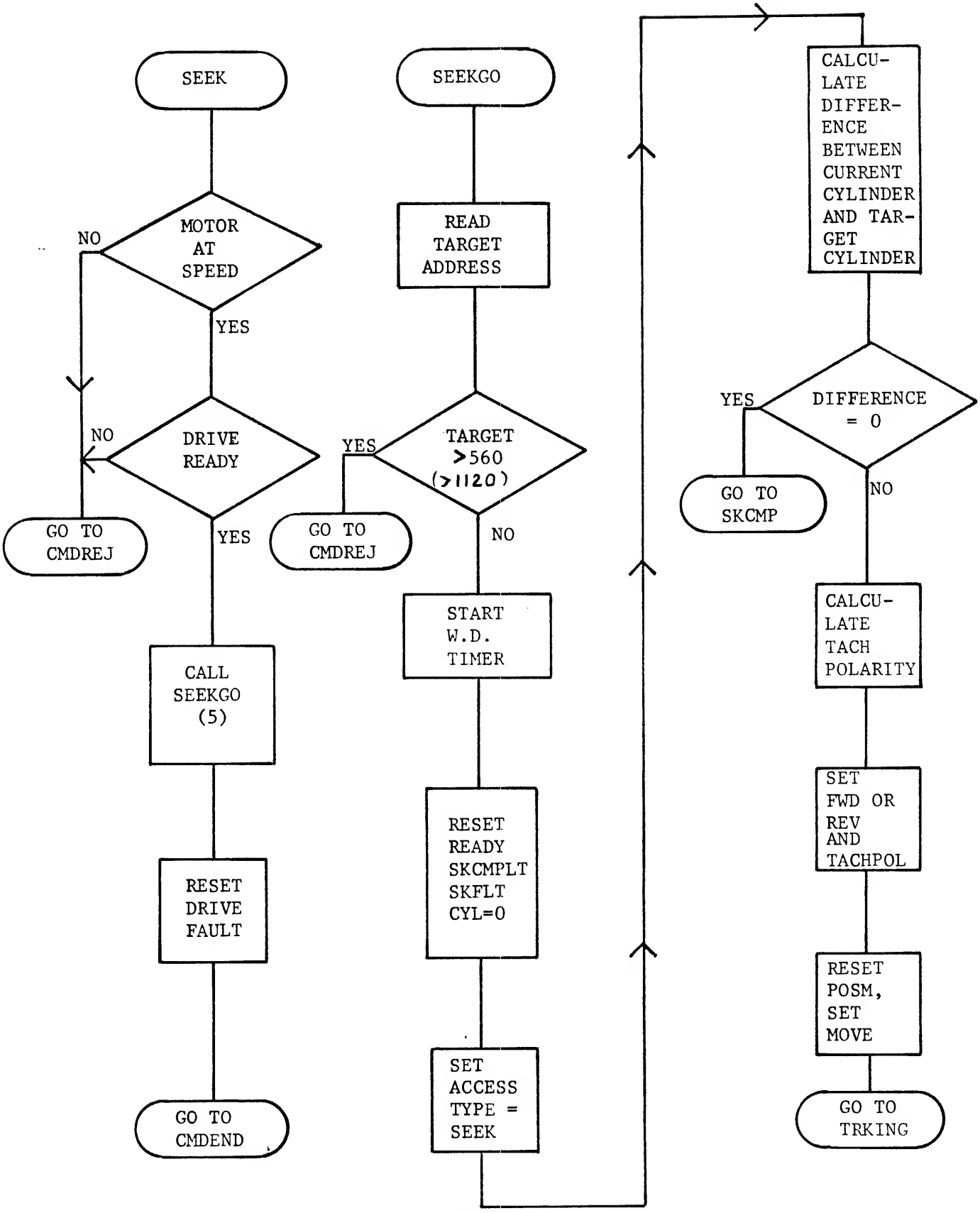



Figure 6.9-7. Seek Operation Flow Chart

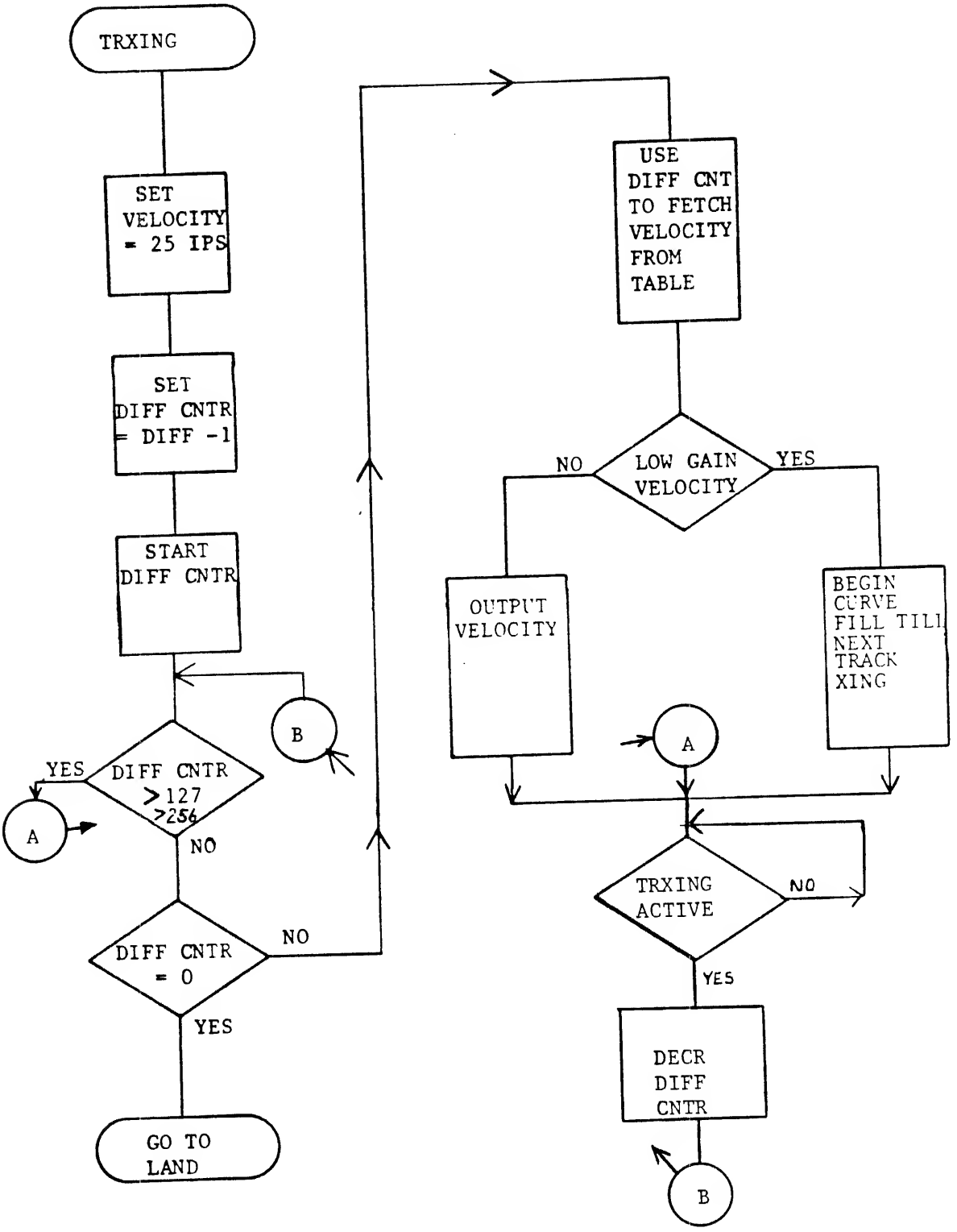



Figure 6.9-8. Track Crossing Flow Chart

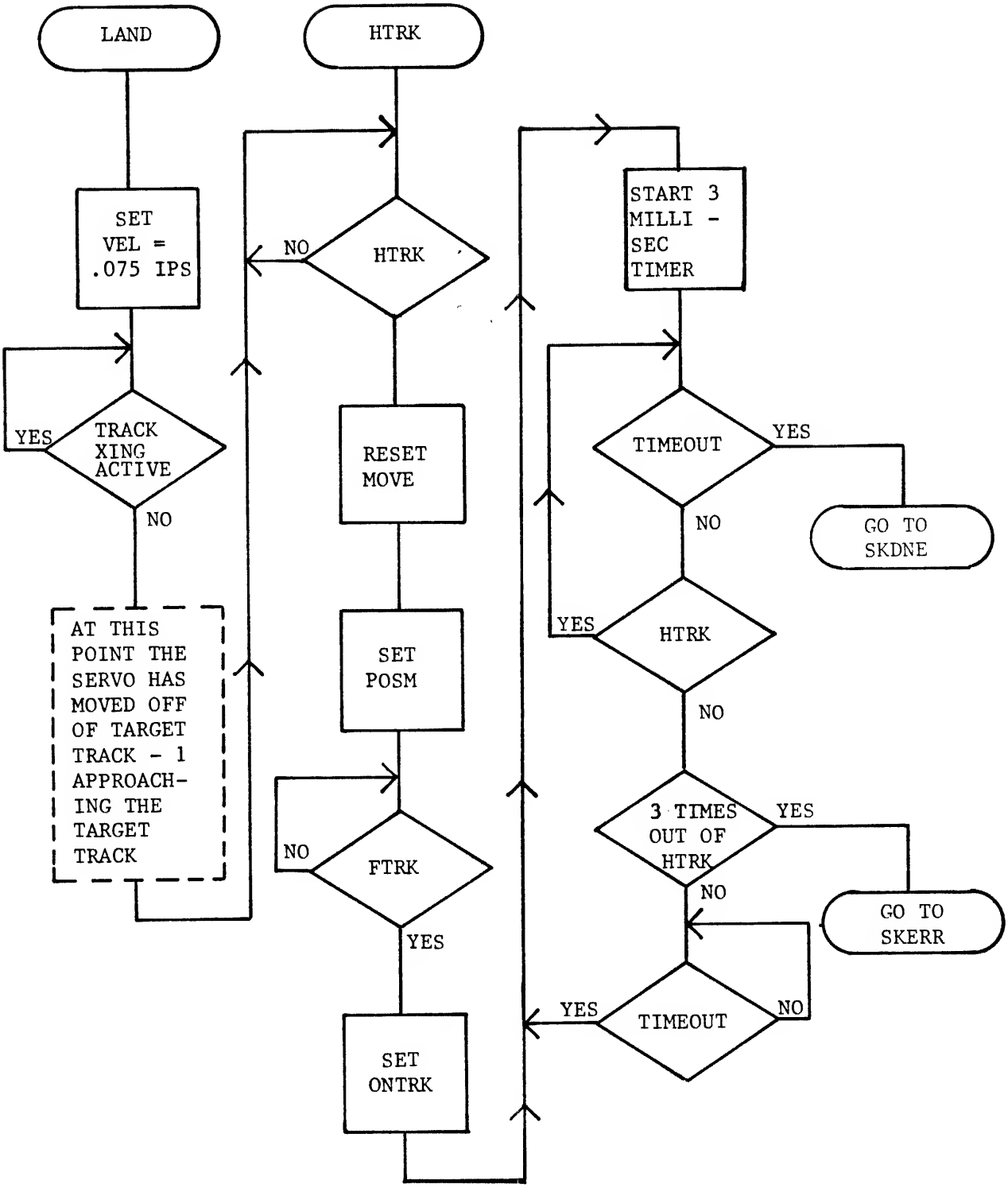



Figure 6.9-9. Land and On Track Flow Chart

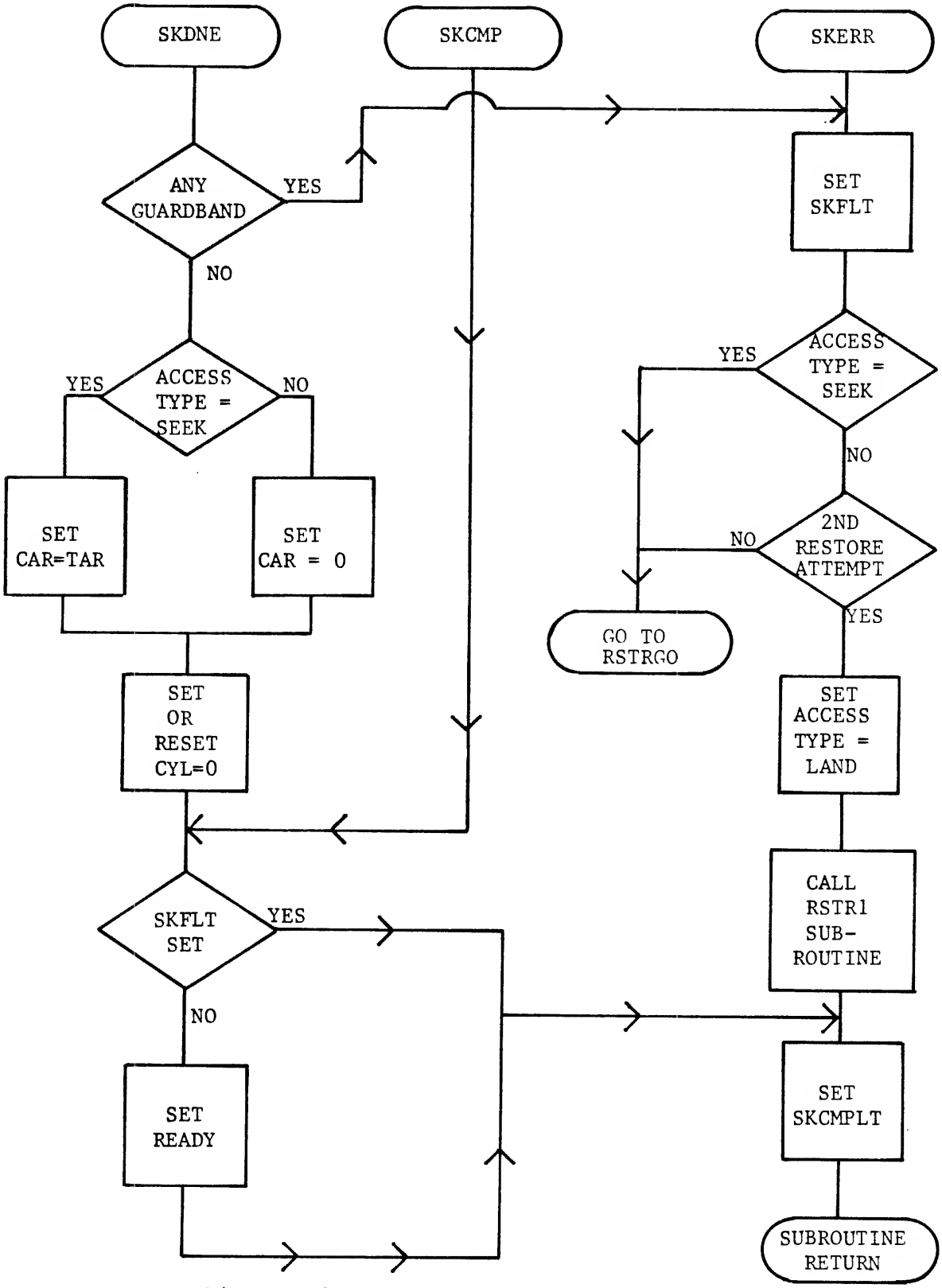



Figure 6.9-10. Seek End Flow Chart

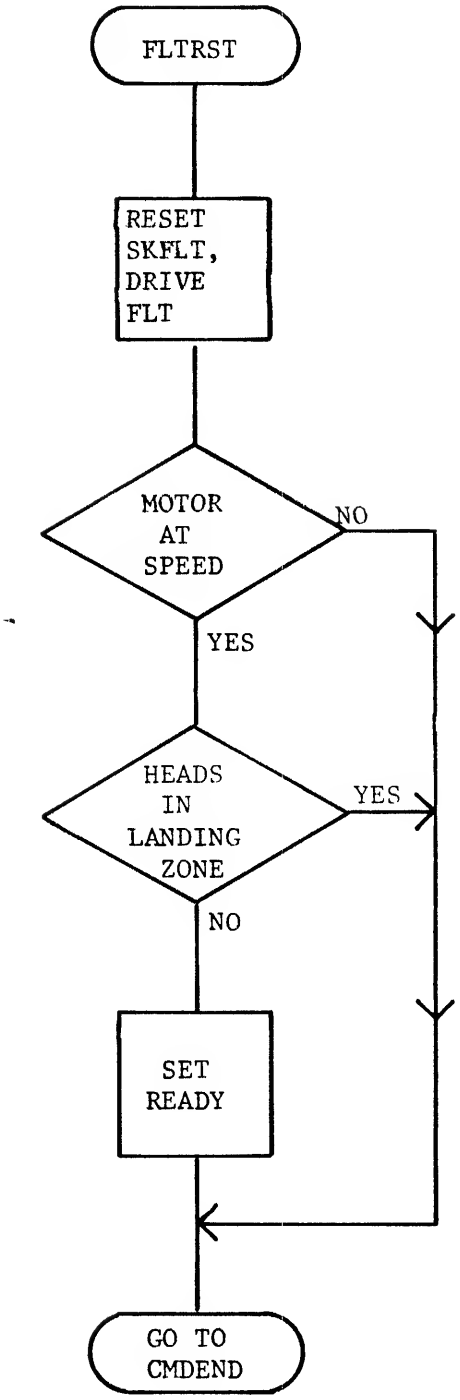



Figure 6.9-11. Fault Reset Flow Chart

# SECTION 7 - TROUBLESHOOTING PROCEDURES

The overall purpose of field service for PRIAM disc drives is to restore system operation by the quickest and most economical means possible. This usually involves replacement of a faulty or suspected assembly with an operational spare. The assembly in question may then be returned to a PRIAM repair depot for component level diagnosis and repair.

Requests for maintenance assistance may be directed to PRIAM's Customer Service Department. PRIAM offers the following services:

1. Telephone Assistance: Service representatives are available (during PRIAM's normal working hours) to assist customers with maintenance, interfacing, and spare parts inquiries.
2. On-site Assistance: PRIAM can provide a factory trained technician to assist the customer's system technician in the testing and repair of PRIAM products.
3. Factory Repair: PRIAM maintains a repair facility at its factory for the convenience of its customers. An entire disc drive, or any repairable assembly, may be returned to PRIAM for repair. Contact PRIAM Customer Service for a return authorization number prior to shipping any drive or assembly to PRIAM.

## 7.1 FIELD ADJUSTMENTS AND PREVENTIVE MAINTENANCE

PRIAM 14-inch disc drives require no field adjustments and no preventive maintenance.

## 7.2 GENERAL INSPECTION

The following checklist may be used as a preliminary procedure to be performed whenever a disc drive is suspected of being faulty:

1. Check that the spindle lock and the head carriage lock are both in the UNLOCK position.
2. Check for proper DC voltages within the disc drive, as described in the OPERATING PROCEDURES section.
3. Check the fuse in the power supply.
4. Check the fuse in the motor control assembly.
5. Check that the device address, write protect, and sector size switches are correctly set, according to the information given in the INSTALLATION section.
6. Check for component discoloration, and for loose or faulty connections.
7. Check and recheck all cable and controller connectors.

If all of the above items seem to be in order, a kind of high-level trouble shooting can be performed, simply by replacing each of the major assemblies one-by-one until the problem disappears. This obviously works best on problems that are stable, as opposed to intermittent. Replacement of the main PCB will confirm the operation of approximately 85% of the electronic circuits in the entire disc drive.

A more symptom-specific approach to troubleshooting is described below in the SYMPTOMS AND CAUSES section.

## 7.3 STATUS AND ERROR CODES

The disc drive is capable of providing quite a bit of information concerning its internal conditions, by means of status indications on the user interface. The exact information available, and the signal lines involved depend on the specific interface used. This is discussed further in the sections describing each individual interface. See also the section on SEEK ERRORS AND FAULT CONDITIONS (below).

## 7.4 SYMPTOMS AND CAUSES

The functions performed by the disc drive fall into the following five categories:

1. Spindle Rotation
2. Command/Status Transfer
3. Head Positioning/Servo
4. Data Write Operations
5. Data Read Operations

In the pages immediately following, symptoms are listed from each of these categories, along with possible causes and the corresponding suggested courses of action.

## SPINDLE ROTATION

| Symptom | Possible Cause | Suggested Action |
|---|---|---|
| Rotation does not start. | Spindle locked. | Place in UNLOCK position. |
| | Incorrect or zero voltage at main PCB connector J3. | Check power supply. |
| | +OFF signal (J4-4) is +5 VDC (should be 0 volts for rotation). | Check microprocessor reset signal on main PCB. Check power-on reset (POR). Check power reset (PRST). All these should be false. |
| | Defective motor control assembly. | Check fuse in motor control assembly. Check LED voltage at J1-5 for the following:<br>+12 VDC on the 3350<br>+4 VDC on the 6650<br>VDC on the 15450 |
| | Defective photocell assembly. | Check for open LED, defective connector or phototransistor. |
| | Defective spindle motor. | Manually rotate spindle in clockwise (viewed from bottom) direction only. If motor is binding, replace entire disc drive. Depot repair is required. |
| Spindle rotates, but stops after about one minute. | Head carriage locked. | Place in UNLOCK position. |
| | Defective motor control assembly. | Replace motor control assembly. |
| | Defective photocell assembly. | Replace photocell assembly. |
| | Speed control not being sensed by microprocessor. | Replace main PCB. |
| | Spindle motor has excessive drag. | Replace entire disc drive (depot repair required). |

SPINDLE ROTATION (continued)

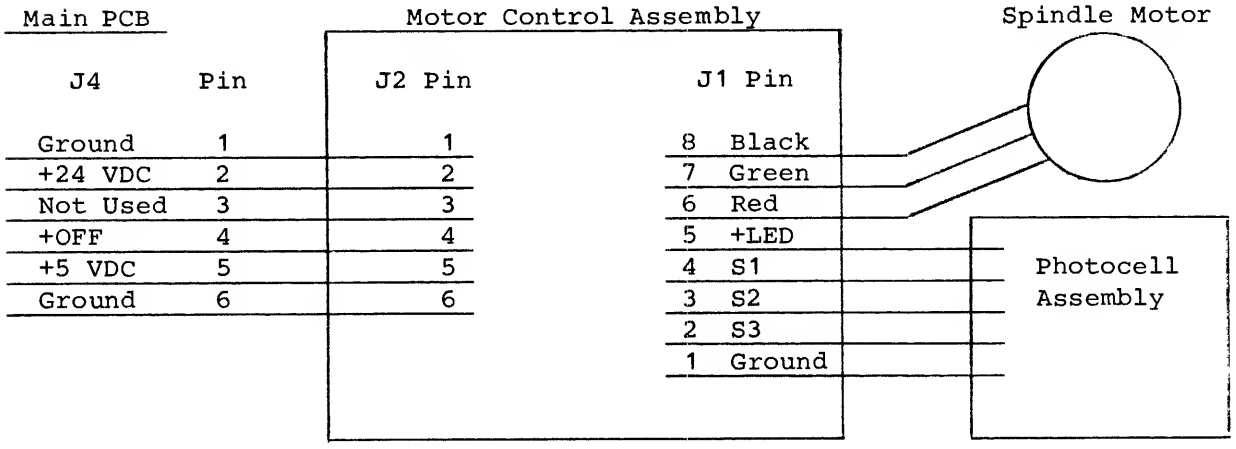
| Symptom | Possible Cause | Suggested Action |
|---|---|---|
| Spindle rotates, but drive does not come Ready, or Ready comes and goes. | Fault condition. | Check Fault status. |
| | Intermittent power supply failure. | Replace power supply. |
| | Defective main PCB. | Replace main PCB. |
| | Defective motor control assembly. | Replace motor control assembly. |
| | Defective head disc assembly. | Replace entire disc drive (depot repair required). |

Comments: Upon completion of power on reset (POR) the microprocessor disables the +OFF signal to the spindle motor. With +OFF at 0 volts the spindle motor should rotate at its specified speed (3100 RPM).

The microprocessor examines Index Marks to determine spindle speed. If the specified spindle speed is not reached within two minutes, the +OFF signal is enabled and spindle rotation is stopped.

Power to the disc drive must be cycled (off and then on) to allow the microprocessor to disable the +OFF signal.

The following diagram shows the connections among the main PCB, motor control assembly, spindle motor, and photocell assembly.



COMMAND/STATUS TRANSFER

| Symptom | Possible Cause | Suggested Action |
|---|---|---|
| Incorrect state on Unit Selected. | Wrong setting on device address switch. | Refer to Section 2.4 for correct switch settings. |
| | Pick and Hold false or Open Cable Detect true (SMD interface only). | Check controller, cable, and connectors. |
| | Unit Select Tag or Unit Address missing or mistimed (SMD interface only). | Check controller, cable, and connectors. |
| Selected drive does not issue status. | Drive not Ready. | See SPINDLE ROTATION (above). |
| | Fault condition. | See FAULT CONDITIONS section (below). |
| | Defective main PCB. | Replace main PCB. |
| Selected drive does not accept commands. | Tag and bus data malfunction (SMD interface only). | Check controller, cable, and connectors. |
| Selected drive issues Fault. | Fault condition. | See FAULT CONDITIONS section (below). |
| Selected drive issues Seek Error. | Defective servo operation. | See HEAD POSITIONING/SERVO (below). |
| Selected drive fails to issue Index. | Defective main PCB. | Replace main PCB. |

Comments: During servo and data write operations, most circuit functions are monitored by the microprocessor. If Ready is true and Fault is false, it is likely that the spindle speed, servo, and data write circuitry are all funtioning in a normal manner.

## HEAD POSITIONING/SERVO

| Symptom | Possible Cause | Suggested Action |
|---|---|---|
| Drive fails to move to new address. | Command transfer circuitry defect. | See COMMAND/STATUS TRANSFER (above). |
| Continuous Seek Error condition. | Defective circuitry. | Defective servo circuitry on main PCB. If fault persists with operational spare, and the fault is not in the spindle speed circuitry, replace the entire disc drive. |
| | Faulty connection to servo read head. | Check connector J6. |
| | Faulty connection to voice coil actuator. | Check connector J5. |
| | Incorrect power voltage. | Check connector J3. Refer to Section 3 for correct voltages. |
| | Head carriage locked. | Place in UNLOCK position. |
| Drive seeks to wrong cylinder. | Inadequate signal from controller. | Check controller, cable, and connectors. |
| | Defective circuitry or servo system. | Defective circuitry on main PCB. If the symptom persists with operational spare, and the fault is not in the controller or cable, replace the entire disc drive. |

Comments: Note that the seek operation may be normal, while the circuitry that checks for correct seek location may be defective.

A large number of symptoms may be associated with malfunctions of the servo circuitry. If servo malfunction is suspected, the recommended procedure is to replace the main PCB. If the head disc assembly is defective, it is highly likely that non-servo related faults (e.g., data errors, failure to come Ready, Fault status true) will also be in evidence.

## DATA WRITE OPERATIONS

| Symptom | Possible Cause | Suggested Action |
|---|---|---|
| Fault is set with each attempt to write data. | Incorrect switch setting or circuit defect. | Verify whether multiple heads have been selected. If this is the case, the following test point will be high:<br>TP__ on the 3350<br>TP__ on the 6650<br>TP__ on the 15450<br><br>Check for the Act Unsafe condition. Act unsafe will be high if there are write transitions with Write Gate false, or no write transitions with Write Gate true.<br><br>See the section on SEEK ERRORS AND FAULT CONDITIONS for other possibilities and corresponding suggested actions. |
| Data is written incorrectly and Fault does not set. | Difficulty in data read operation. | See DATA READ OPERATIONS (below). |

## DATA READ OPERATIONS

| Symptom | Possible Cause | Suggested Action |
|---|---|---|
| Drive fails to read, but will write without a Fault. | Defect in read circuitry. | Check all cable connections.<br>Replace terminator.<br>Replace main PCB. |
| Drive reads data fields and header fields correctly, but will not read newly written data. | Difficulty in data write operation. | See DATA WRITE OPERATIONS (above). If Fault is set during write operation, see the section on SEEK ERRORS AND FAULT CONDITIONS. |

Comments: If read errors persist after replacement of the terminator and the main PCB, and if the cable connections are correct, it is possible that the format being used is erroneous.

If the format is correct, replacement of the entire disc drive is recommended.

TEST POINT CHART 14" (200149-SMD)

| TEST POINT | TYPE LOCK | ORIGIN | DESCRIPTION | LOC | GND | WAVE FORM |
|---|---|---|---|---|---|---|
| TP1 | TSTR Alog | Read Amp | +Analog MFM Data (To TP5) | 2E3 | C | |
| TP2 | GROUND | | Ground "C" (with TP1 & TP5) | 2F3 | | |
| TP3 | ECL Digital | Read Amp | Digitized Read Data | 2E9 | C | 30 |
| TP4 | ECL Digital | I/O | READ GATE | 2C7 | C | |
| TP5 | TSTR Alog | Read Amp | -Analog MFM Data (with TP1) | 2F3 | C | |
| TP6 | | | VCO Feedback | 2B6 | C | |
| TP7 | ECL Digital | uP Cntl | +SYNC | 2C7 | C | |
| TP8 | ECL Digital | uP Cntl | ENABLE | 2D6 | C | |
| TP9 | ECL Digital | Read Dly | DATA (Data Sep) | 3F6 | C | |
| TP10 | ECL Digital | Data Sep | NRZ Read Data | 3F4 | C | |
| TP11 | ECL Digital | VFO Cntl | +Phase Error (VFO)(with TP14) | 2C5 | C | |
| TP12 | ECL Digital | MUX | DATA (Read MUX Output) (PLO) | 2C6 | C | |
| TP13 | ECL Digital | VFO | Data Window | 3F6 | | |
| TP14 | ECL Digital | VFO Cntl | -Phase Error (VFO)(with TP11) | 2C5 | C | |
| TP15 | OpAmp Analog | VFO Cntl | VFO Control Voltage | 2B4 | C | 33 |
| TP16 | GROUND | | Ground "C" (VFO Ref) | 2C4 | | |
| TP17 | | | PLO Correction Voltage | 3D2 | B | 4 |
| TP18 | ECL Digital | MFM Encdr | +WRT CLK (MFM Write Data) | 3E2 | | |
| TP19 | TTL Digital | | -Phase Error (PLO with TP26) | 3D4 | B | |
| TP20 | | | | | | |
| TP21 | OpAmp Digital | R/W Drvr | +ACT UNSAFE | 1D2 | B | |
| TP22 | GROUND | | Ground "B" | 3C1 | | |
| TP23 | | | | | | |
| TP24 | | | | | | |
| TP25 | OpAmp Digital | Head Sel | +MULTI SEL (Head Bias) | 1C2 | B | |
| TP26 | TTL Digital | | +Phase Error (PLO with TP19) | 3D4 | B | |
| TP27 | | | | | | |
| TP28 | TTL Digital | PLO Error | +MSB — 2 (To PLO Error Det) | 3D5 | B | |
| TP29 | TTL Digital | PLO Cntr | +MSB | 3C7 | | 3 |
| TP30 | OpAmp Analog | Servo Amp | AGC'D Servo Data (Carrier) | 5F3 | D | 1 |
| TP31 | OpAmp Digital | Servo Car | Sync Detect | | D | 2 |
| TP32 | OpAmp Analog | Servo Pos | Servo Position Peak B | 4D5 | D | 5 |
| TP33 | OpAmp Analog | Servo Pos | Servo Position Peak A | 4D5 | D | 5 |
| TP34 | OpAmp Analog | Servo Vel | TRKXING Filler | 5C7 | D | |
| TP35 | TTL Dig | uP Cntl | +MOVE (High During Seek) | 5B6 | D | 10-15,22 |
| TP36 | OpAmp Analog | Servo Pos | Position Demod | 4D4 | D | 10-16,20 |
| TP37 | | | | | | |
| TP38 | | | | | | |
| TP39 | TTL Dig | Servo HTK | +Inihibit Differentiators | 5B6 | | |
| TP40 | OpAmp Analog | POS | Position Signal | 4D3 | | 10-16,20 |
| TP41 | D/A Analog | uP D/A | +CURVE D/A (Target Velocity) | 6E3 | | 16 |
| TP42 | GROUND | H-SW Servo | Ground "E" (H-SW) | 5D1 | | |
| TP43 | | | | | | |
| TP44 | OpAmp Alog | H-Sw Servo | IR (Voice Coil Current) | 5C2 | E | 17,18 |
| TP45 | OpAmp Analog | H-SW | Velocity (from Coil Current) | 4A4 | D | 24 |
| TP46 | OpAmp Analog | Velocity | Servo Error (To H-SW Error) | 5E6 | E | 23,26 |
| TP47 | OpAmp Analog | POS | Filtered Position | 4D3 | D | 10-16,20 |
| TP48 | OpAmp A/D | POS | TACH Differentiator Out (DXA) | 4B3 | | 19 |
| TP49 | OpAmp Analog | H-SW | Velocity In Tach | 4B5 | D | |
| TP501 | TTL Dig | INTF | SECTOR MARK | 8D4 | | 35,36 |
| TP502 | TTL Dig | INTF | READY · BUSY (to D Rdy) | 8C3 | | |
| TP503 | TTL Dig | Servo SD | INDEX | 4F3 | B | 34 |

TEST POINT CHART 14 INCH DISK (200173-PRIAM)

| TEST POINT | TYPE LOCK | ORIGIN | DESCRIPTION | LOC | GND | WAVE FORM |
|---|---|---|---|---|---|---|
| TP1 | Tstr Analog | Rd Preamp | +Analog MFM Data (with TP5) | 2E3 | C | |
| TP2 | GROUND | Rd Preamp | Ground "C" Read Preamp | 2F3 | | |
| TP3 | ECL Digital | Rd Limit | Digitized Read Data (MFM) | 2E8 | C | 30 |
| TP4 | ECL Digital | Rcvr | +Read Gate (to Read Mux) | | C | |
| TP5 | Tstr Analog | Rd Preamp | -Analog MFM Data with TP1) | 2F3 | C | |
| TP7 | ECL Digital | Wr Clk | +Sync (Delay 9 bytes) | 2C7 | | |
| TP9 | ECL Digital | Data Sep | Data (into Data Sep) | 3E6 | C | |
| TP10 | ECL Digital | Data Sep | NRZ Read Data | 3F3 | C | |
| TP13 | ECL Digital | VFO | Data Window (Separator) | 3F6 | C | |
| TP15 | OpAMP Alog | VFO | VFO Control Voltage | 2B3 | C | 33 |
| TP16 | GROUND | VFO | Ground "C" for TP15 | 2C4 | | |
| TP17 | OpAmp Alog | PLO | PLO Correction Voltage | | B | 4 |
| TP18 | ECL Digital | MFM Ecdr | +WRT CLK (MFM Write Data) | 3E4 | C | |
| TP20 | GROUND | R/W | Ground "A" R/W Heads | 1E5 | | |
| TP21 | OpAmp Digit | R/W Drvr | +Act Unsafe (not latched!) | 1D2 | B | |
| TP22 | GROUND | PLO | Ground "B" (for TP17) | 3C2 | | |
| TP25 | OpAmp Digit | R/W Heads | +MultiSel (bias to 2 heads) | 1C2 | B | |
| TP28 | TTL Dig | uP Expdr | +FWD ( | | | |
| TP29 | TTL Digital | PLO Cntr | +MSB (PLO divided by 32) | 3B6 | D | 3 |
| TP30 | OpAmp Alog | Servo Amp | AGC'D Servo Data (Carrier) | 5F3 | D | 1 |
| TP35 | TTL Digital | uP Expndr | +Move (high during seek) | 5B6 | D | 10-15,22 |
| TP36 | OpAmp Alog | Servo Pos | Position Demod (Peak Det) | 4D4 | D | 10-16,20 |
| TP40 | OpAmp Alog | Servo Pos | Position Signal ( | 4D3 | D | 10-16,20 |
| TP41 | OpAmp Alog | uP D/A | +Curve D/A (Target Velocity) | 6E3 | D | |
| TP42 | GROUND | Servo H-sw | Ground "E" (H-Switch) | 5D1 | | |
| TP44 | OpAmp Alog | Servo H-Sw | Motor Current (to Voice Coil) | 5C2 | E | 17,18 |
| TP45 | OPamp Alog | Servo H-Sw | Velocity (from Coil Current) | 4A5 | D | 24 |
| TP46 | OpAmp Alog | Servo H-SW | Servo Error (to H-Switch) | 5E6 | E | 23,26 |
| TP47 | OpAmp Alog | Servo Pos | Filtered Position | 4D2 | D | 10-16,20 |
| TP48 | oPAmp Alog | Servo Pos | Tach Differentiator Out | 4B2 | D | 19 |
| TP50 | | | | | | |
| TP51 | TTL Digital | uP Expndr | -PSYC (to PLO Corrector | 3A5 | B | 37 |
| TP501 | TTL Digital | uP Cntr | Sector Mark | 8D4 | H | 35,36 |
| TP502 | TTL Digital | Status | Ready & not Busy (to DRDY) | 8C3 | | |

## TEST POINT CHART 14 INCH ANALOG BOARD (200214)

| TEST PIN | TYPE LOGIC | ORIGIN | DESCRIPTION | LOC | GND | WAVE FORM |
|---|---|---|---|---|---|---|
| (CHIP SOCKET LOCATION IS 16F ON ANALOG PCB) | | | | | | |
| Pin 1 | OpAmp Alog | Servo S/H | POSN (Filtered Position) | 5D1 | D | 10-16,20 |
| Pin 2 | OpAmp Alog | D/A Curve | D/A (Analog Target Velocity) | 7B1 | D | 16 |
| Pin 3 | TTL Dig | uProc | -POSN (Position Mode) | 8D1 | | |
| Pin 4 | OpAmp Alog | OnTrack | COMP | 7B1 | D | |
| Pin 5 | Ref | Servo | BODE 1 (Ref 24K) | 5D1 | D | |
| Pin 6 | Ref | Servo | BODE 2 (Ref 1K) | 5D1 | D | |
| Pin 7 | | | | | | |
| Pin 8 | OpAmp Alog | Servo S/H | POS (Position Demod) | 5E1 | D | 10-16,20 |
| Pin 9 | GROUND | | GROUND "D" | 5C1 | | |
| Pin 10 | OpAmp Alog | D/A Curve | CRV (Sw Target Vel) | 7A1 | | |
| Pin 11 | OpAmp Alog | Servo Pos | DXB (Differentiated Position) | 6D1 | D | |
| Pin 12 | TTL Dig | uProc | -FWD (Same as TP22) | 8E1 | D | |
| Pin 13 | OpAmp Alog | AGCC uP | GC (Analog AGC from D/A) | 7F1 | D | |
| Pin 14 | Analog | H-Switch | IR (Voice Coil Current) | 7B1 | D | 17,18 |
| Pin 15 | OpAmp | Servo Pos | VD | 6E1 | D | |
| Pin 16 | OpAmp Alog | Voice Coil | VEL (Integral of IR) | 6D1 | D | 24 |

## TEST POINT CHART 14 INCH SPLIT SMD (200264)

| | | | | | |
|---|---|---|---|---|---|
| TP1 | TTL Dig | Alog Bd | INDEX | 4D3 | 34 |
| TP2 | TTL DIG | Decoder | SECTOR MARK | 4E3 | 35,36 |

## TEST POINT CHART 14 INCH SPLIT PRIAM (200209)

| | | | | | |
|---|---|---|---|---|---|
| TP1 | TTL Dig | Alog Bd | INDEX | 3D3 | 34 |
| TP2 | TTL Dig | Decoder | SECTOR MARK | 3E4 | 35,36 |
| TP3 | TTL Dig | Busy FF | BUSY FF | 1A7 | |

TEST POINT CHART 14" ANALOG (200214)
15450

| TEST POINT | SIGNAL TYPE | ORIGIN | DESCRIPTION | LOC | GND | WAVE FORM |
|---|---|---|---|---|---|---|
| TP1 | Tstr Analog | Read Amp | +Analog Read Data (with TP3) | 2F3 | C | |
| TP2 | GROUND | | Ground "C" (Read Amp Ref) | 2F3 | | |
| TP3 | Tstr Analog | Read Amp | -Analog Read Data (with TP1) | 2E3 | C | |
| TP4 | ECL Dig | Read Amp | Digitized Read Data (MFM) | 3F8 | C | 30 |
| TP5 | ECL Dig | I/O | +Sync | 3B8 | | |
| TP6 | ECL Dig | Data Sep | NRZ Read Data (To XMTRS) | 4F3 | C | |
| TP7 | ECL Dig | Read Amp | Data (MFM Data to Separator) | 4E5 | C | |
| TP8 | ECL Dig | RCVR | Read Gate A (To MUX) | 3C8 | C | |
| TP9 | ECL Dig | Read Amp | Data (Data or PLO to VFO) | 3D6 | C | |
| TP10 | ECL Dig | Clocks | ENABLE (Sync Read Gate) | 3B7 | C | |
| TP11 | ECL Dig | VFO | VCO Feedback (VFO) | 3C5 | C | |
| TP12 | ECL Dig | VFO Div | Data Window | 4F5 | C | |
| TP13 | GROUND | | Ground "C" (For VFO Ref) | 3C4 | | |
| TP14 | Tstr Analog | VFO Cntl | VFO Error (R40 to Gnd "C") | 3C3 | C | |
| TP15 | OpAmp Alog | VFO Cntl | VFO Correction Voltage | 3F4 | C | 33 |
| TP16 | ECL Dig | | | | | |
| TP17 | GROUND | | Ground "A" | 2C1 | | |
| TP18 | OpAmp Dig | Head Sel | +Multi Sel | 2B1 | F | |
| TP19 | OpAmp Dig | Head Wr | +Act Unsafe | 2C1 | F | |
| TP20 | TTL Dig | Servo Pos | -TRKXING | 6E2 | D | |
| TP21 | OpAmp Analog | PLO Cntl | PLO Correction Voltage | 6B5 | D | 4 |
| TP22 | | | | | | |
| TP23 | | | | | | |
| TP24 | OpAmp Analog | Servo Amp | Carrier | 5E5 | D | 1 |
| TP25 | OpAmp Dig | Servo Amp | SD (Sync Detect) | 5F1 | D | 2 |
| TP26 | | | | | | |
| TP27 | | | | | | |
| TP28 | TTL Dig | PLO Cntl | +PLO Error (to PLO,TP21) | 6A7 | F | |
| TP29 | TTL Dig | Servo Pos | -FTRK (±100u" Offtrack) | 6F2 | D | |
| TP30 | | | | | | |
| TP31 | TTL Dig | Servo Pos | -HTRK (±500u" Offtrack) | 6E2 | D | |
| TP32 | OpAmp Alog | | | 6E2 | D | |
| TP33 | TTL Dig | | FWD ODD (Clocked by Move) | 6E5 | D | |
| TP34 | | Servo Data | GB1 (Guardband near Data) | 6C6 | F | |
| TP35 | | Servo Data | GB2 (Head Landing Zone) | 6B6 | F | |
| TP36 | TTL Dig | PLO Cntl | -PLO Error (to PLO,TP21) | 6A7 | F | |
| TP37 | | Servo Data | INDEX (unshaped) | 6C6 | F | |

## 7.5 SEEK ERRORS AND FAULT CONDITIONS

Seek errors result when a head does not lock on the target track. Whenever a seek error occurs, the drive's track counter is reset to zero. This is done automatically by restoring the head to cylinder zero. The fault must be reset, and a new seek command may then be issued.

The Seek Error indication will be set true whenever the microprocessor detects any of the following conditions:

1. Seek Incomplete (track following servo unable to lock onto track within the prescribed time).
2. Restore or Rezero not completed within the prescribed time.
3. Invalid seek address detected (SMD, ANSI and B4 inerfaces only).
4. Guardband Error (servo head has entered the guardband area).

When the microprocessor detects one of these conditions, it issues an internal Restore or Rezero command, which returns the head to cylinder 000 and sets a Seek Error Latch. The Seek Error Latch must be cleared by a Fault Reset, Restore or Rezero command issued to the drive by the user.

The exact manner in which the Seek Error indication appears on the user interface depends on which interface option is present. See the individual interface description sections for details.

Fault status is set, Ready is disabled, and writing of data is inhibited whenever the safety circuitry on the main PCB detects a Fault conditon. The following list discusses the possible origins of such a conditon, and suggests what remedial actions could be taken in each case:

1. Write Gate true with Write Protect switch ON (or Write Enable switch OFF).

   Check switch for correct setting.

2. Act Unsafe (Write gate without Write Current or Write Current without Write Gate).

   If the fault is isolated to an individual head, then (with power off) check the head assembly for continuity. If the head assembly is faulty, return the entire disc drive to a repair depot.

   If the fault occurs on all heads, replace the main PCB.

3. Multiple heads selected (only one data head should be selected at a given time).

   Check the center tap of each data head. Only one data head should have +7 VDC.

   If more than one data head center tap is at +7 VDC, replace the main PCB.

4. Write Gate and Read Gate both true at the same time.

   Check the controller for proper operation and the interface cable for the proper connections.

   If the problem persists, replace the main PCB.

5. Write Gate true, but heads not precisely located over the designated cylinder.

   Replace the main PCB.

   If the problem persists, replace the entire disc drive.

6. No seek request, but head movement is detected.

   Replace the main PCB.

   If the problem persists, replace the entire disc drive.

7. The PLO signal is not synchronized.

   Replace the main PCB.

   If the problem persists, replace the entire disc drive.

8. Spindle rotation is outside of specification.

   Check the motor control assembly for a defective component.

   Check the photocell assembly for a defective connection, LED, or phototransistor.

   Check the power supply for a defective connection, DC voltage level, or component.

   If the fault can not be corrected by replacing the motor control assembly, photocell assembly, and power supply, then replace the entire disc drive.

9. More than one control tag is active (SMD and B4 interfaces only).

   Check controller, cable, and procedures.

   If the problem persists, replace the main PCB.

If any of conditions 6, 7, or 8 (above) are detected, the microprocessor will attempt a restore to cylinder 000.

Any of the following measures will reset Fault status:

1. Power On Reset -- remove and reapply DC power.
2. Fault Clear -- Tag 3 and Bit 4 on interface "A" or BUS cable (SMD and B4 interfaces).
3. Fault Reset command (PRIAM and ANSI interfaces).
3. Ground potential at J8-2.

# SECTION 8 - ASSEMBLY REPLACEMENT PROCEDURES

All of the replaceable assemblies in a PRIAM disc drive may be removed and replaced using standard hand tools. It is highly recommended that maintenance personnel use the assembly replacement approach to field service, rather than attempting component level repair.

## 8.1 PRECAUTIONS

1. Always make sure that the head lock and spindle lock levers are both in the LOCK position before the drive is moved in any way.
2. Always make sure that the power is off when removing or reinserting any printed circuit boards or connectors.
3. Use proper size screwdrivers, wrenches, and other tools. Keep track of the screws and other parts you remove, and use the same hardware when reinstalling each assembly.
4. Use properly calibrated test equipment.
5. Keep accurate records of all observations made during servicing.

Before attempting to remove any assemblies, make sure that both the spindle lock and head lock levers are in the LOCK position. The spindle lock engages the fan on the spindle motor shaft. To lock it, rotate the spindle clockwise (as viewed from the bottom) until the teeth of the lock can fit onto the blades of the fan. The head lock is a wire lever, which should be pulled out, then turned to the LOCK position. If it does not turn easily, gently lift the far end of the drive so that the head carriage will return to the fully retracted position. Then turn the lever to LOCK.

## 8.2 HEAD DISC ASSEMBLY

The head disc assembly (HDA) is a sealed contamination-resistant enclosure containing all moving parts in the disc drive. It should not be opened for any reason. If the HDA is defective, the entire disc drive should be returned to a qualified repair depot. Do not remove the HDA from the frame assembly.

## 8.3 PHOTOCELL ASSEMBLY

The photocell assembly is mounted on the bottom of the motor spindle. To remove the photocell assembly, first unplug the connector at the motor control assembly. Then remove the two mounting screws, which can be accessed through the holes provided in the perforated cover over the bottom of the spindle. When you install the replacement board, be sure to locate the LEDs in exactly the same location relative to the shutters.

## 8.4 MOTOR CONTROL ASSEMBLY

The motor control assembly is mounted on the bottom of the frame. To remove the motor control assembly, first unplug the two connectors. Then remove the three mounting bolts and release the two plastic retainers.

## 8.5 MAIN PCB

The main PCB is mounted on the top of the frame. To remove it, first unplug all the connectors, carefully noting their positions and orientations for later replacement. Then remove the eight mounting screws.

Extreme care should be taken in removing the IC connectors, especially those going to the head disc assembly. Gently pry the connectors off, using a suitable size slender screwdriver. If the connectors to the HDA are broken, it will be necessary to replace the entire disc drive.

## 8.6 POWER SUPPLY

The power supply may be mounted separately from the disc drive, or it may be mounted on the bottom of the frame. If it is mounted separately, simply unplug the power connector. If it is mounted in the frame, unplug the connector and then remove the power supply mounting screws.

## SECTION 9 - SPARE PARTS LIST

Replaceable assembly part numbers are given below. Additonal part number information (and/or a bill of material listing for customers establishing depot repair) is available from PRIAM Customer Service.

| | | |
|---|---|---|
| Head Disc Assembly (3350) | 330330 | |
| Head Disc Assembly (6650) | 330410 | |
| Head Disc Assembly (15450) | 331003 | |
| Photocell Assembly | 200053 | |
| Motor Control Assembly | 200083 | |
| Main PCB (PRIAM Interface) | 200113 (OLD) | 200173 (NEW) |
| Main PCB (SMD Interface) | 200088 (OLD) | 200148 (NEW) |
| Main PCB (ANSI Interface) | | |
| Main PCB (Basic Four Interface) | 200098 | |
| Frame Assembly | 330397 | |
| 15450 Split PRIAM Interface | 200208 | |
| 15450 Analog PCB | 200213 | |
| 15450 Split SMD Interface | 200263 | |
| Power Supply (3350) | 330358 | |
| Power Supply (6650) | 330352 | |
| Power Supply (15450) | | |
| Power Cord | 101116 | |
| Mounting Slides (3350) | 330143 | |
| Mounting Slides (6650) | 330183 | |
| Mounting Slides (15450) | | |
| Terminator (PRIAM Interface) | 200133 | |
| Terminator (SMD Interface) | 200128 | |
| Terminator (ANSI Interface) | | |
| Terminator (Basic Four Interface) | 200138 | |

Orders for spare parts may be placed with your PRIAM Sales Representive or with PRIAM Customer Service at the factory.

# SECTION 10 - PRIAM INTERFACE

10.1 **PRIAM Interface.** PRIAM offers a basic 8-bit bidirectional bus control interface designed to be readily connected to popular 8-bit and 16-bit microprocessors. Across this interface all spindle and head positioning controls are passed.

Read and write data is passed via synchronous serial-bit NRZ signal lines. The interface provides INDEX, SECTOR MARK, READ/REFERENCE CLOCK, and WRITE CLOCK signals.

Up to four drives may be daisy chained along a single 50-conductor flat ribbon cable. Power is provided via a separate connector. Control switches are provided on the PCB.

10.2 **Connectors and Pin Assignments.** All drive signal connections are made via a single 50-pin ribbon cable connector. A second 50-pin connector is available for daisy chaining to another drive or for a terminator for the last drive in the string. Up to four drives may be daisy chained.

A separate connector for DC power is provided. However, if the PRIAM optional power supply is used, then its output is connected to this DC power connector and AC power must be supplied to the optional power supply.

Mini-dip switches are provided on the PCB to select drive address, sector length, write protect functions, and write clock control.

**1 Interface Connectors.** The interface connectors are 50-pin ribbon cable connectors, and provide for interface cable and terminator connections. The pins are numbered 1 through 50. A recommended mating connector is Spectra Strip 802-050-004 or Scotchflex 3425-0000. The lines (at the drive end) are described below.

**PRIAM Interface Connector**

| Pin | Signal Name | Line Type |
|---|---|---|
| 1 | Ground | Ground |
| 2 | + DBUS 0 | Bidirectional/Single |
| 3 | + DBUS 1 | Bidirectional/Single |
| 4 | + DBUS 2 | Bidirectional/Single |
| 5 | + DBUS 3 | Bidirectional/Single |
| 6 | + DBUS 4 | Bidirectional/Single |
| 7 | + DBUS 5 | Bidirectional/Single |
| 8 | + DBUS 6 | Bidirectional/Single |
| 9 | + DBUS 7 | Bidirectional/Single |
| 10 | Ground | Ground |
| 11 | - READ GATE | Received/Single |
| 12 | Ground | Ground |
| 13 | - RESET | Received/Single |
| 14 | Ground | Ground |
| 15 | - WRITE GATE | Received/Single |
| 16 | Ground | Ground |
| 17 | - RD Received/Single | |
| 18 | - WR Received/Single | |
| 19 | + AD 1 | Received/Single |
| 20 | + AD 0 | Received/Single |
| 21 | Ground | Ground |
| 22 | - DRIVE SELECT 1 | Received/Single |
| 23 | - DRIVE SELECT 2 | Received/Single |
| 24 | - DRIVE SELECT 3 | Received/Single |
| 25 | - DRIVE SELECT 4 | Received/Single |
| 26 | Ground | Ground |
| 27 | Ground | Ground |
| 28 | + 5 VCD (Terminator Box) | Diode OR'ed/Single |
| 29 | - HEAD SELECT 4 | Received/SIngle |
| 30 | - HEAD SELECT 2 | Received/Single |
| 31 | - HEAD SELECT 1 | Received/Single |
| 32 | Ground | Ground |
| 33 | - INDEX | Transmitted/Single |
| 34 | Ground | Ground |
| 35 | - READY | Transmitted/Single |
| 36 | Ground | Ground |
| 37 | - SECTOR MARK | Transmitted/Single |
| 38 | Ground | Ground |
| 39 | + WRITE DATA | Received/DIFF |
| 40 | - WRITE DATA | Received/DIFF |
| 41 | Ground | Ground |
| 42 | + WRITE CLOCK | Received or Transmitted/DIFF |
| 43 | - WRITE CLOCK | Received or Transmitted/DIFF |
| 44 | Ground | Ground |
| 45 | + READ/REFERENCE CLOCK | Received or Transmitted/DIFF |
| 46 | - READ/REFERENCE CLOCK | Received or Transmitted/DIFF |
| 47 | Ground | Ground |
| 48 | + READ DATA | Transmitted/DIFF |
| 49 | + READ DATA | Transmitted/DIFF |
| 50 | Ground | Ground |

2. DC Power Connector

This connector is used to supply DC power to the drive. It is a 6-pin AMP MATE-N-LOK connector, and the recommended mating connector is an AMP 1-480270-0 socket with AMP 60617-1 pins.

DC POWER CONNECTOR

| PIN | VOLTAGE |
|---|---|
| 1 | Ground |
| 2 | +24 VDC |
| 3 | -5 VDC |
| 4 | -12 VDC |
| 5 | +5 VDC |
| 6 | Ground (+24V Return) |

3. AC Power Connector

This is a 3-pin connector used to supply AC power to the disc drive when the PRIAM optional power supply is used. The mating connector is a Belden 5PH-386 or equivalent.

AC POWER CONNECTOR

| PIN | VOLTAGE |
|---|---|
| L | 110 or 220 VAC (HOT) |
| E | Frame Ground |
| N | 110 or 220 VAC (COMMON) |

4. Remote Panel Connector

This is an 8-pin DIP socket connector. It provides limited remote sensing and control as described below.

REMOTE PANEL CONNECTOR

| PIN | SIGNAL NAME |
|---|---|
| 1 | - WRITE PROTECT (CONTROL) |
| 2 | - FAULT RESET (CONTROL) |
| 3 | - READY (STATUS) |
| 4 | Ground |
| 5 | - BUSY (STATUS) |
| 6 | - FAULT (STATUS) |
| 7 | Reserved |
| 8 | + 5 VDC |

10.3 **Interface Signal Descriptions.** This section gives functional description for the signals on the 50-pin interface connector.

**1 +DBUS 0-7.** This high-active 8-bit wide bus is used to transfer commands and status (head carriage control and interface) between the disc drive and the controller. These lines connect directly to an 8304B (or 8286) bus transceiver, as shown in Figure 10.4-1. DC characteristics are listed in Table 10.4-1. These lines should be terminated at each end.

**2 +AD 0-1.** This high-active 2-bit wide address bus is used to select one of three registers into which data can be stored, or one of three registers from which data can be read. These lines connect directly to a 74LS244 Schmitt-triggered receiver gated by DRIVE SELECTED, as shown in Figure 10.4-2. The DC characteristics are listed in Table 10.4-2. These lines should be terminated at the drive end.

**3 –RD.** This low-active signal is used to gate the contents of the selected register (decode of AD1, AD0) onto the DBUS. This line is connected to a 74LS244, gated by DRIVE SELECTED, as shown in Figure 10.4-2. The DC characteristics are listed in Table 10.4-2. This line should be terminated at the drive end.

**4 –WR.** This low-active signal is used to gate the DBUS into the selected register (decode of AD1, AD0). This line is connected to a 74LS244, gated by DRIVE SELECTED, as shown in Figure 10.4-2. The DC characteristics are listed in Table 10.4-2. The DC characteristics are listed in Table 10.4-2. This line should be terminated at the drive end.

**5 –RESET.** This low-active signal resets the drive logic. If the drive is sequenced down when RESET occurs, it will remain sequenced down. If the drive is sequenced up, it will remain up and the head carriage will Restore to cylinder zero. This line is connected to 74LS244, gated by DRIVE SELECTED, as shown in Figure 10.4-2. The DC characteristics are listed in Table 10.4-2. This line should be terminated at the drive end.

**6 –DRIVE SELECT 1-4.** These low-active signals (decoded) enable drive response. No readying, writing, register selection, or command response will occur unless the drive is selected. These lines are connected to single-ended receivers, as shown in Figure 10.4-3. The DC characteristics are listed in Table 10.4-3. This line should be terminated at the drive end.

**7 –HEAD SELECT 1, 2, and 4.** These low-active signals are used to select the desired data head for reading or writing. Head selection decoding is shown in Table . This line is connected to a 74LS244, gated by DRIVE SELECTED, as shown in Figure 10.4-2. The DC characteristics are listed in Table 10.4-2. This line should be terminated at the drive end.

**8 –READY.** This low-active signal from the drive indicates that the drive is up to speed and ready to read, write, or seek. This line is driven by a 75462 open collector driver, as shown in Figure 10.4-4. The DC characteristics are listed in Table 10.4-4. This line must be terminated at the controller end.

**9 –INDEX.** This low-active signal occurs once per revolution and indicates the beginning of a track. This line is driven by a 75462 open collector driver, as shown in Figure 10.4-4. The DC characteristics are listed in Table 10.4-4. This line must be terminated at the controller end.

**10 –SECTOR MARK.** This low-active signal indicates the beginning of a sector. This line is driven by a 75462 open collector driver, as shown in Figure 10.4-4. The DC characteristics are listed in Table 10.4-4. This line must be terminated at the controller end.

**11 –WRITE GATE.** This low-active signal enables the writing of data by a selected head. This line is connected to a 74LS244, as shown in Figure 10.4-2. The DC characteristics are listed in Table 10.4-2. This line should be terminated at the drive end.

**12 –READ GATE.** This low-active signal initiates synchronization of the drive's phase lock loop for data separation. READ GATE must be enabled during a gap. This line is connected to a 74LS244, as shown in Figure 10.4-2. The DC characteristics are listed in Table 10.4-2. This line should be terminated at the drive end.

**13 +, –WRITE DATA.** WRITE DATA is an NRZ serial data signal synchronous with WRITE CLOCK. WRITE DATA is received by an RS422 type differential line receiver as shown in Figure 10.4-5. The DC characteristics are listed in Table 10.4-5.

**14 +, −WRITE CLOCK.** This signal is switch selectable. It can be a square wave signal from the controller which is phased locked to the WRITE DATA, or (if the switch is in the other position) it can be a square wave signal from the drive to the controller to provide clocking and synchronization for WRITE DATA. The controller should be designed so that WRITE DATA is stable at the drive connector during the negative transition of WRITE CLOCK. WRITE CLOCK is received by an RS422 type differential line receiver, as shown in Figure *10.4-5* The DC characteristics are listed in Table *10.4-5* These lines should be terminated. If long cables are used, cable delays must be considered.

**15 +, −READ/REFERENCE CLOCK.** This square wave signal provides clocking and synchronization for reading and writing data. It is derived from either the servo clock or the VFO synchronized to the READ DATA signal. It is driven by an RS422 type differential driver, as shown in Figure *10.4-6* The DC characteristics are listed in Table *10.4-5*.

**16 +, −READ DATA.** This serial NRZ signal is used to transmit data from the drive to the controller. This output is valid 9 microseconds after READ GATE is enabled. It is driven by an RS422 type differential drivers, as shown in Figure *10.4-6* The DC characteristics are listed in Table *10.4-5*.

Of the above signals, there are several that are used specifically to facilitate serial data transfer between the disc drive and the controller. These are described below, with some additional details.

1. *INDEX* The INDEX pulse occurs whenever the servo track index mark is encountered, to indicate the beginning of a track.

2. *READY* The READY signal indicates that the selected drive is ready to read, write, or seek. When READY is false, the controller should not initiate WRITE, READ, or SEEK commands. However, READY will go false when a SEEK command is initiated. READY will later go true when the head carriage is positioned on the specified cylinder, if no fault condition exists.

3. *SECTOR MARK* The SECTOR MARK pulse occurs at the beginning of each sector (sector size is selectable by setting the mini-switches on the read/write digital PCB).

4. *HEAD SELECT 1, 2, and 4* These low-active signals are gated by DRIVE SELECTED, and are used to select the data head, as shown in Table *10.3-1*.

Table 10.3-1. Head Selection

| Head Select 1 | Head Select 2 | Head Select 4 | Selected Head 3350 6650 | 15450 |
|---|---|---|---|---|
| High | High | High | Zero | Zero |
| Low | High | High | One | One |
| High | Low | High | Two | Two |
| Low | Low | High | Zero* | Three |
| High | High | Low | Zero* | Four |
| Low | High | Low | One* | Five |
| High | Low | Low | Two* | Six |
| Low | Low | Low | Zero* | Zero* |

* = Selected by default because of the number of heads available.

5. *WRITE GATE* WRITE GATE when active, enables data to be written on the disc. READY must be true before WRITE GATE is activated. Any attempt to write between INDEX and the first SECTOR MARK will result in a DRIVE FAULT, because the prerecorded skip defect information is write protected. DRIVE FAULT will also be set if any of the following conditions occur during a write operation.

**Drive Fault Conditions**

1. WRITE GATE without write current at the head
2. Write current at the head without WRITE GATE
3. WRITE GATE without READY
4. More than one head selected
5. No transitions during write
6. WRITE GATE with WRITE PROTECT
7. Spindle speed error
8. RESET while drive is Sequenced Up
9. Off-Track condition when track following (READY true)
10. Failure to Restore
11. Software Error (time out of watch dog timer)

6. *WRITE CLOCK* WRITE CLOCK provides clocking and synchronization for WRITE DATA. The controller generates WRITE CLOCK by echoing the READ/REFERENCE CLOCK signal back to the drive, with suitable phase delay relative to WRITE DATA.

7. *WRITE DATA* WRITE DATA provides the data to be stored on the disc. NRZ (non-return-to-zero) data is required for WRITE DATA. READ/REFERENCE CLOCK (received from the drive) is used by the controller to clock WRITE DATA on the positive edge. READ/REFERENCE CLOCK is retransmitted back to the drive as WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe WRITE DATA into the drive's encoder circuitry.

8. *READ GATE* READ GATE must be enabled in a gap area (all 0s recorded), and at least 9 microseconds before the sync byte. READ GATE enables the VFO clock to synchronize with the information from the read head. Activating READ GATE during a data record may cause the VFO to spuriously lock in an incorrect phase relationship for decoding the recorded information. Six microseconds after the leading edge of READ GATE, the internal READ CLOCK signal is enabled to the READ/REFERENCE CLOCK interface signal lines.

9. *READ/REFERENCE CLOCK* READ/REFERENCE CLOCK provides clocking and synchronization for reading and writing data. When READ GATE is not active, READ/REFERENCE CLOCK is switched to the PLO clock, which is phased locked to the servo signal. A change in the phase of READ/REFERENCE CLOCK will occur when it is switched between the servo and VFO clocks.

10. *READ DATA* Data from the drive is in serial NRZ (non-return-to-zero) form, and is synchronized with READ/REFERENCE CLOCK after a microsecond delay from the leading edge of READ GATE. READ DATA may not be valid for the first 9 microseconds after READ GATE is enabled.

10.4 **Interface DC Characteristics.** This section, through tables and figures, sets forth the details that need to be observed, in order to properly transmit and receive the interface signals. The signal characteristics are shown in Table 10.4-1 to 10.4-5 and Figures 10.4-1 to 10.4-6

**Table 10.4-1 DBUS Transceiver DC Characteristics**

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{OL}$ | Output Low Level | | 0.5 | V | $I_{OL}$ = 32 mA |
| $V_{OH}$ | Output High Level | 2.4 | | V | $I_{OL}$ = −5 mA |
| $I_{OFF}$ | Output Off Current | | −0.2 | mA | $V_{OFF}$ = 0.45 V |
| | | | +0.2 | mA | $V_{OFF}$ = 5.25 V |
| $V_{IL}$ | Input Low Level | | 0.9 | V | |
| $V_{IH}$ | Input High Level | 2.0 | | V | |

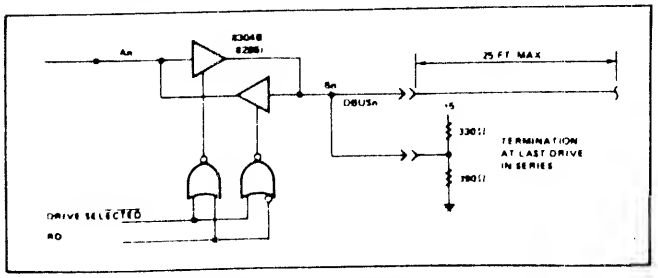



**Figure 10.4-1 DBUS Transceiver**

### Table 10.4-2 Single End Line Receiver Gated by DRIVE SELECTED Characteristics

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level | 2.0 | | V | |
| $V_{IL}$ | Input Low Level | | 0.8 | V | |
| $I_{IH}$ | High Level Input Current | | 0.02 | mA | $V_I = 2.7$ V |
| $I_{IL}$ | Low Level Input Current | | −0.2 | mA | $V_I = 0.4$ V |

Cable connections should be terminated at the last drive.

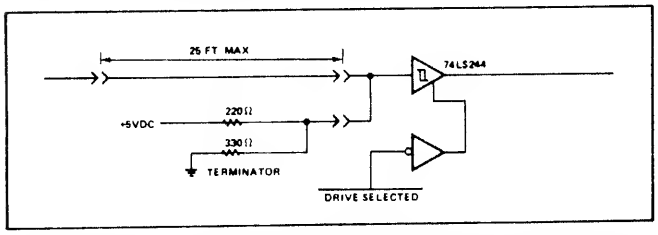



**Figure 10.4-2 Single End Line Receiver Gated By DRIVE SELECT**

### Table 10.4-3 Single End Line Receiver DC Characteristics

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{T+}$ | Positive-going Threshold | 1.4 | 1.9 | V | |
| $V_{T-}$ | Negative-going Threshold | 0.5 | 1.0 | V | |
| $I_{IH}$ | High Level Input Current | | 0.02 | mA | $V_I = 2.7$ V |
| $I_{IL}$ | Low Level Input Current | | −0.2 | mA | $V_I = 0.4$ V |

Cable connections should be terminated at the last drive.

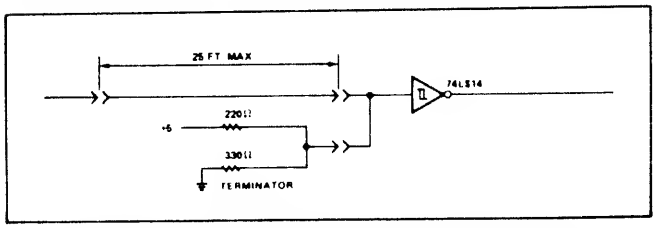



**Figure 10.4-3 Single End Line Receiver**

### Table 10.4-4 Single End Line Driver DC Characteristics

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $I_{OH}$ | High Level Output Current | | 0.1 | mA | |
| $I_{OL}$ | Low Level Output Current | 300 | | mA | |
| $V_{OH}$ | High Level Output Voltage | 2.4 | | V | |
| $V_{OL}$ | Low Level Output Voltage | | 0.8 | V | $I_{OL} = 300$ mA |

This line must be terminated at the controller end.

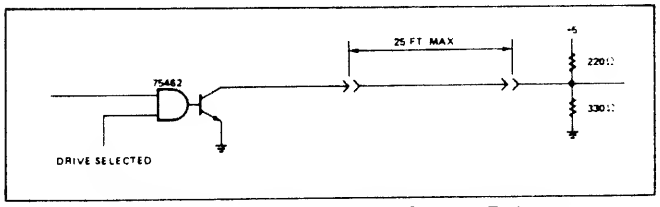



**Figure 10.4-4 Single End Line Driver**

### Table Differential Line Receiver DC Characteristics

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{TH}$ | Differential Input High Threshold | | 0.2 | V | |
| $V_{ICR}$ | Common Mode Input Range | ±15 | | V | |
| $I_{I(REC)}$ | Reveiver Input Current | | 2.3 | mA | |

**Table 10.4-6 Differential Line Driver DC Characteristics**

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | High Level Output Voltage | 2.5 | | V | $I_{OH} = -20$ mA |
| $V_{OL}$ | Low Level Output Voltage | | 0.32 | V | $I_{OL} = 20$ mA |
| $I_{OZ}$ | Output Off Current | | ±0.2 | mA | |
| $I_{OH}$ | High Level Output Current | | −20 | mA | |
| $I_{OL}$ | Low Level Output Current | | +20 | mA | |
| $I_{OS}$ | Short Circuit | −30 | −150 | mA | |

Note: The last drive in a string should be terminated.

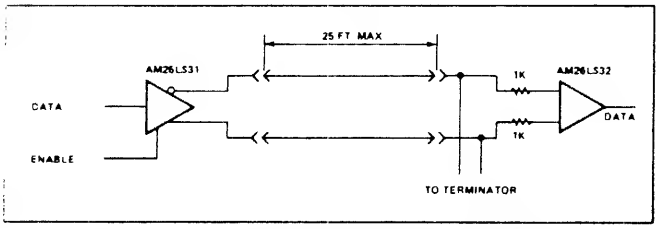



**Figure 10.4-5 Differential Line Drivers and Receivers**

10.5 **Interface Timing.** This section discusses the timing requirements for the various operations performed on the controller interface.

1. *Register Load Timing* Register load timing is shown in Figure 10.5-1 The AC characteristics are listed in Table 10.5-1.

**Table 10.5-1 Register Load AC Characteristics**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AW}$ | Address stable before WR | 60 | | ns |
| $t_{WA}$ | Address hold time for WR | 30 | | ns |
| $t_{WW}$ | WR pulse width | 100 | | ns |
| $t_{DW}$ | Data set up time for WR | 60 | | ns |
| $t_{WD}$ | Data hold time for WR | 30 | | ns |
| $t_{RV}$ | Recovery time between WR | 200 | | ns |

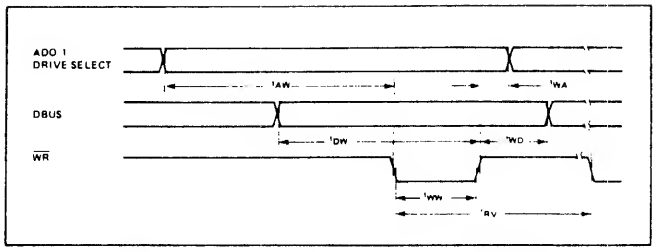



**Figure 10.5-1 Register Load Timing**

2. *Register Read Timing* Register read timing is shown in Figure 10.5-2 The AC characteristics are listed in Table 10.5-2

**Table 10.5-2 Register Read AC Characteristics**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AR}$ | Address stable before RD | 60 | | ns |
| $t_{RA}$ | Address hold time for RD | 30 | | ns |
| $t_{RR}$ | RD pulse width | 100 | | ns |
| $t_{RD}$ | Data delay from RD | | 60 | ns |
| $t_{DF}$ | RD to data floating | 10 | 40 | ns |

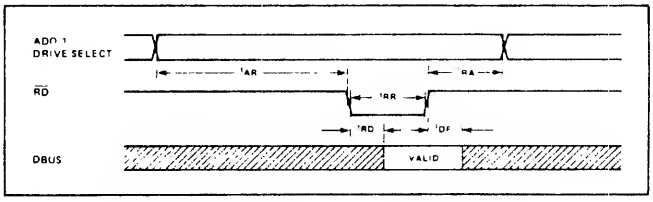



**Figure 10.5-2 Register Read Timing**

3. *Reset Timing* Reset timing is shown in Figure 10.5-3 The AC characteristics are listed in Table 10.5-3

**Table 10.5-3 Reset AC Characteristics**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{RST}$ | RESET pulse width | 100 | | ms |
| $t_{SR}$ | DRIVE SELECT TO RESET | 0 | | ns |

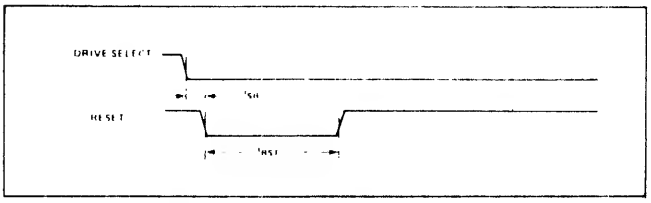



**Figure 10.5-3 Reset Timing**

4. *INDEX AND SECTOR MARK Timing* INDEX and SECTOR MARK timing is shown in Figure 10.5-4 The AC characteristics are listed in Table 10.5-4.

### Table 10.5-4 INDEX and SECTOR MARK AC Characteristics

| Symbol | Parameter | Timing | Units |
|---|---|---|---|
| $t_{IW}$ | INDEX pulse width | 1.92 ± .19 | µs |
| $t_{IR}$ | INDEX period | 19.35 ± .5 | ms |
| $t_{SW}$ | SECTOR MARK pulse width | 960 ± 140 | ns |
| $t_{IS}$ | INDEX to first SECTOR | 30.7 ± 4.7 | µs |
| $t_{BYTE}$ | Byte period | 960 ± 144 | ns |

$t_{SR}$ = Sector width = (Sector size in bytes) x ($t_{BYTE}$) ± 10%

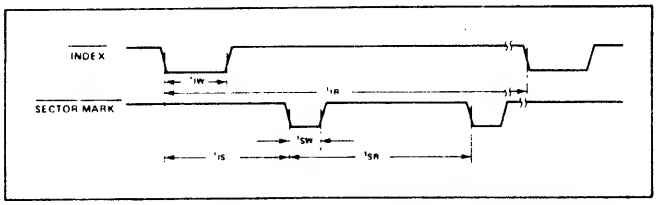



**Figure 10.5-4 INDEX and SECTOR MARK Timing**

5. *WRITE DATA and WRITE CLOCK Timing* WRITE DATA and WRITE CLOCK timing is shown in Figure 10.5-5 The AC characteristics are listed in Table 10.5-5

### Table 10.5-5 WRITE DATA and WRITE CLOCK AC Characteristics

| Symbol | Parameter | Timing | Units |
|---|---|---|---|
| $t_{CLK}$ | WRITE CLOCK period | 120 ± 18 | ns |
| $t_{WH}$ | WRITE CLOCK high pulse width | 60 ± 9 | ns |
| $t_{WL}$ | WRITE CLOCK low pulse width | 60 ± 9 | ns |
| $t_{BIT}$ | WRITE DATA bit period | 120 ± 18 | ns |
| $t_{DC}$ | WRITE DATA setup time | 20 * | ns min |
| $t_{CD}$ | WRITE DATA hold time | 20 * | ns min |
| $t_{BYTE}$ | Byte period | 960 ± 144 | ns |
| * | 60 ns typical | | |

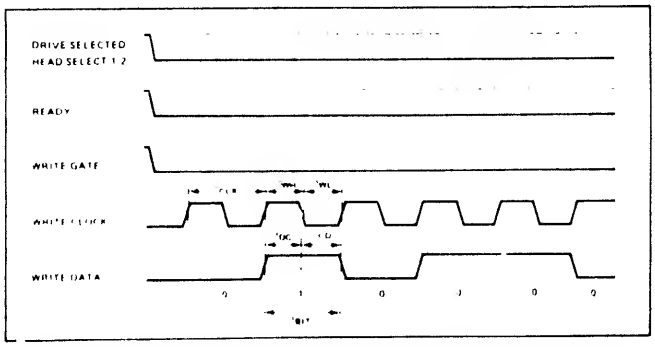



**Figure 10.5-5 WRITE DATA and WRITE CLOCK Timing**

6. *READ DATA and READ CLOCK Timing* READ DATA and READ CLOCK timing is shown in Figure 10.5-6 The AC characteristics are listed in Table 10.5-6

### Table 10.5-6 READ DATA and READ CLOCK AC Characteristics

| Symbol | Parameter | Timing | Units |
|---|---|---|---|
| $t_{CLK}$ | READ CLOCK period | 120 ± 18 | ns |
| $t_{WH}$ | READ CLOCK high pulse width | 60 ± 9 | ns |
| $t_{WL}$ | READ CLOCK low pulse width | 60 ± 9 | ns |
| $t_{BIT}$ | READ DATA bit period | 120 ± 18 | ns |
| $t_{DC}$ | READ DATA setup time | 40 * | ns min |
| $t_{CD}$ | READ DATA hold time | 40 * | ns min |
| $t_{BYTE}$ | Byte period | 960 ± 144 | ns |
| * | 60 ns is typical | | |

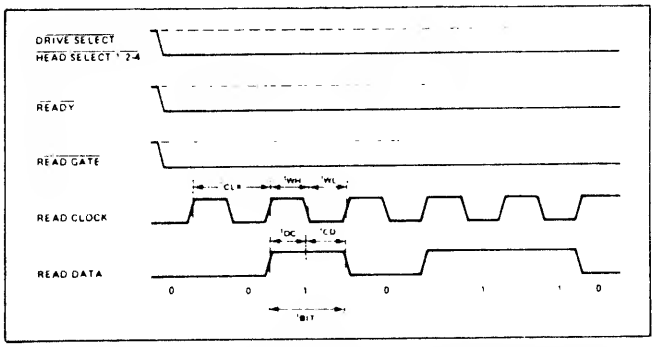



**Figure 10.5-6 READ DATA and READ CLOCK Timing**

7. *Record Writing* Figure 10.5-7 shows the timing requirement for writing full sectors (ID and data fields) and also writing data fields only. The AC characteristics are listed in Table 10.5-7

**Table 10.5-7 Record Writing Control AC Characteristics**

| Symbol | Parameter | Timing | Units |
|---|---|---|---|
| $t_{SH}$ | DRIVE SELECTED to HEAD SELECTED | 20 | µs min |
| $t_{SR}$ | DRIVE SELECTED to READY | 100 | ns min |
| $t_{SG}$ | SECTOR MARK to WRITE GATE | 0 ± 1 | µs min |
| $t_{IDG}$ | ID gap timing | 23 | bytes min |
| $t_{IDF}$ | ID fill | 2 | bytes min |
| $t_{DG}$ | Data gap (no write-to-read transitions) | 11 | bytes min |
| $T_{DF}$ | Data fill | 2 | bytes min |
| $t_{HW}$ | HEAD SELECTED OR WRITE GATE | 100 | ns |
| $t_{BYTE}$ | Byte period | 960 ± 144 | ns |

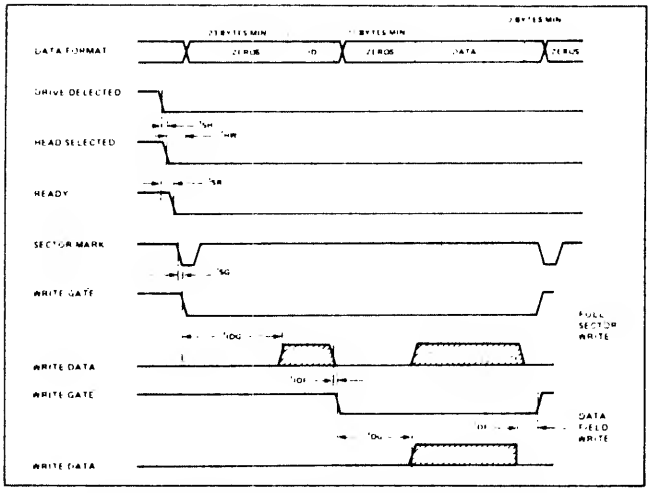



**Figure 10.5-7 Record Writing Timing**

8. *Record Reading* Figure 10.5-8 shows the timing requirements for reading full sectors (ID and data fields) and also for reading data fields only. The AC characteristics are listed in Table 10.5-8

**Table 10.5-8 Record Reading Control AC Characteristics**

| Symbol | Parameter | Timing | Units |
|---|---|---|---|
| $t_{SH}$ | DRIVE SELECTED to HEAD SELECTED | 20 | µs |
| $t_{SR}$ | DRIVE SELECTED to READY | 100 | ns min |
| $t_{RDLW}$ | READ GATE delay for gaps allowing write-to read transitions | 13 | µs min |
| $t_{RDLR}$ | READ GATE delay for gaps limited to read-to-read or read-to-write transitions | 1.9 | µs min |
| $t_{SYN}$ | Read PLO synchronization (data not valid during this period) | 9 | µs min |
| $t_{HR}$ | HEAD SELECTED to READ GATE | 25 | µs min |
| $t_{BYTE}$ | Byte period | 960 ± 144 | ns |

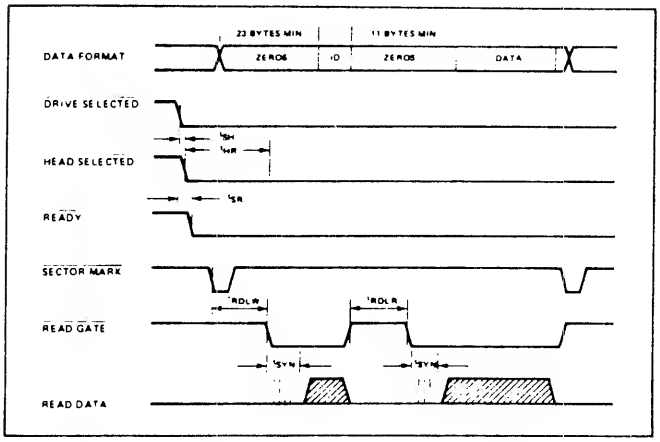



**Figure 10.5-8 Record Reading Timing**

The combined operations are shown in Figure 10.5-9

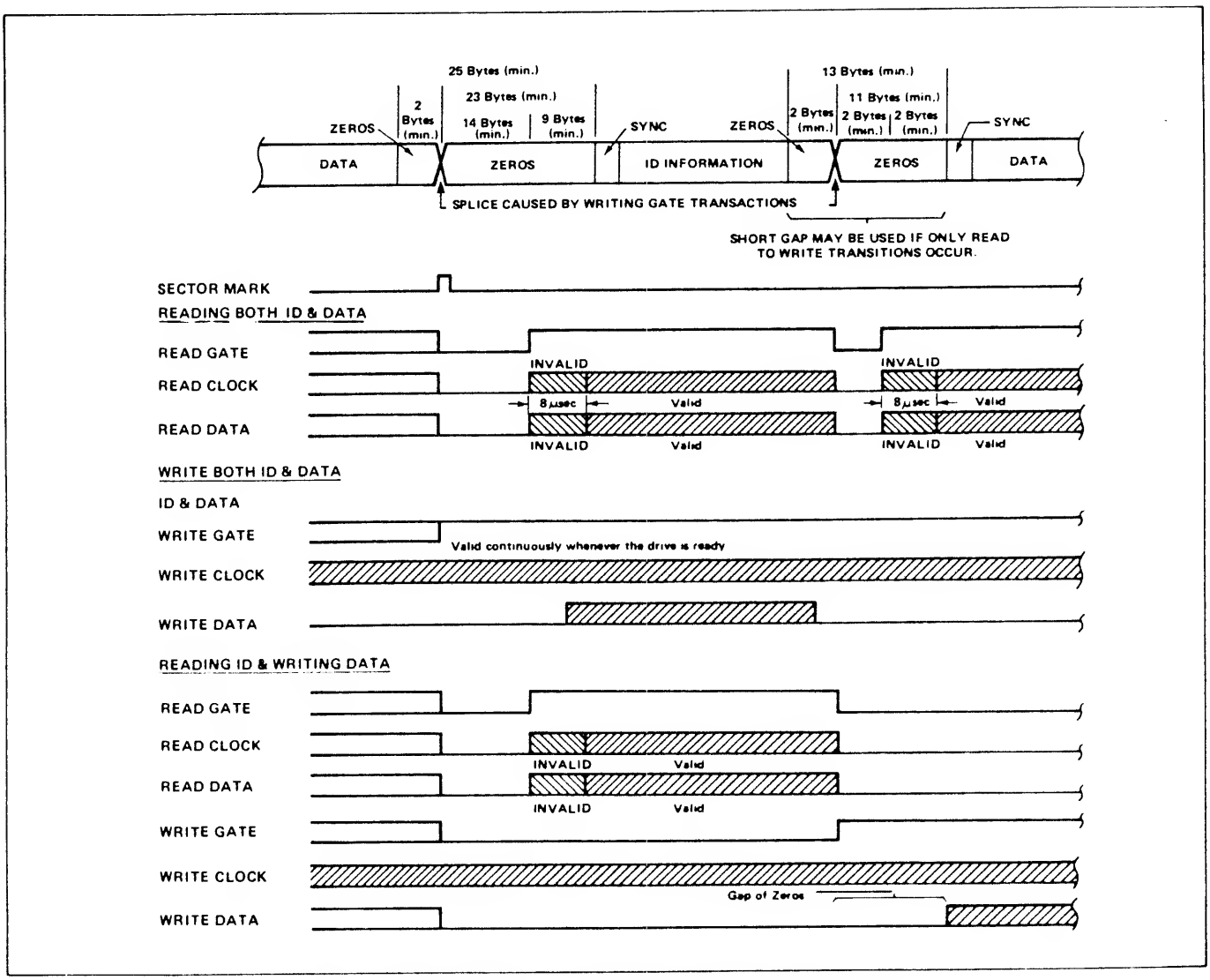



**Figure 10.5-9 Read and Write Transitions During Gap**

10.6 **User-Accessible Registers.** The user (controller) sends control commands and target cylinder addresses to the disc drive via the eight bidirectional bus lines DBUS 0-7. The disc drive sends status information and current cylinder address information to the controller via these same eight lines. DBUS 0-7 is a tri-state bus, and thus these lines present an open circuit to the controller's data bus unless they have been activated by DRIVE SELECT. An active DRIVE SELECT combined with an active WR enables the drive's line receivers on DBUS 0-7, so that the information on the bus can be written into the drive's three control registers. An active DRIVE SELECT combined with an active RD enables the drive's line drivers on DBUS 0-7, so that the information in the drive's three status-like registers can be returned to the controller. The following six registers are involved:

The COMMAND REGISTER receives and stores commands from the controller.

The TARGET ADDRESS REGISTER—UPPER BYTE receives and stores the two or three most significant bits of the desired cylinder address.

The TARGET ADDRESS REGISTER—LOWER BYTE receives and stores the eight least significant bits of the desired cylinder address.

The STATUS REGISTER holds current drive status information.

The CURRENT ADDRESS REGISTER—UPPER BYTE holds the two or three most significant bits of the current cylinder address.

The CURRENT ADDRESS REGISTER—LOWER BYTE holds the eight least significant bits of the current cylinder address.

The registers are accessed by activating the appropriate combinations of address lines A1 and A0, and the WR or RD signal, as shown in Table 10.6-1. Note that the command and target address registers are write-only, while the status and current address registers are read-only.

**Table 10.6-1 Register Selection.**

| RD | WR | A1 | A0 | Selected Register |
|---|---|---|---|---|
| 0 | 1 | 0 | 0 | Command Register |
| 0 | 1 | 0 | 1 | Target Address—Upper Byte |
| 0 | 1 | 1 | 0 | Target Address—Lower Byte |
| 1 | 0 | 0 | 0 | Status Register |
| 1 | 0 | 0 | 1 | Current Address—Upper Byte |
| 1 | 0 | 1 | 0 | Current Address—Lower Byte |

Note: 1 = Active, 0 = Inactive.

10.7 **Commands.** Table 10.7-1 lists the command codes for the valid commands. The commands are discussed individually following Table

**Table 10.7-1 Command Code Summary.**

| | DBUS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Command Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Sequence Up | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Sequence Down | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Restore | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Seek | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Fault Reset | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| Read Drive ID | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Read Bytes/Sector | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

**Sequence Up.** The Sequence Up command causes the disc drive spindle motor to power up. The rotational speed of the disc is monitored, and after the drive is up to speed, the heads are positioned to cylinder zero. The drive presents BUSY status (BUSY bit set in the status register) while Sequence Up is in process. At the successful completion of Sequence Up, BUSY is cleared and CYLINDER ZERO, SEEK COMPLETE, and READY are set. If Sequence Up is unsuccessful, WRITE PROTECT and DRIVE FAULT are set.

**Sequence Down.** The Sequence Down command causes the heads to be positioned to the landing zone, and the spindle motor to be braked to a stop. WRITE PROTECT status is set at the completion of Sequence Down.

**Restore.** The Restore command causes the head carriage to be positioned to cylinder zero. The drive Restores automatically on Sequence Up, or when a SEEK FAULT is detected. If the Restore command is unsuccessful, the heads will be positioned to the landing zone, and DRIVE FAULT status will be set. If the drive is not sequenced up, the Restore command will function as a Sequence Up Command.

**Seek.** The Seek command causes the drive to seek to a specified cylinder. Prior to issuing the Seek command, the controller must place the desired cylinder address in the target address registers. Upon receipt of the Seek command, the drive clears READY status and sets BUSY, while moving the head carriage to the correct cylinder. When this has been done, the drive sets READY and also sets SEEK COMPLETE status. If the Seek command is unsuccessful, the drive Restores to cylinder zero, and sets READY, CYLINDER ZERO, and SEEK FAULT status.

**Fault Reset.** The Fault Reset command clears the two fault conditions—SEEK FAULT and DRIVE FAULT.

**Read Drive ID.** The Read Drive ID command loads the drive ID into the lower byte of the current address register, and clears READY status. The controller may then retrieve the information by reading the lower byte of the current address register. The values of the ID code for various PRIAM disc drives are given in Table 3-18.

After the DRIVE ID information has been read by the controller, a Sequence Up or Restore command must be issued to bring the drive back to the READY state. In general, the current address registers contain the current cylinder address if the drive is READY, and the last requested parameter information if the drive is not READY.

**Read Bytes per Sector.** The Read Bytes per Sector command loads the number of bytes per sector into the current address registers, and clears READY status.

As with the Read Drive ID command, a Sequence Up or Restore command must be issued to bring the drive back to the READY state.

**Table 10.7-2 Drive ID Assignments**

| ID Code (Hex) | Drive Designation | |
|---|---|---|
| 00 | Not Valid | |
| 01 | DISKOS 3350-10 or 3350-10 | (20,160 bytes/track) |
| 02 | DISKOS 3350-01 | (19,960 bytes/track) |
| 03 | DISKOS 3450 | (12,960 bytes/track) |
| 04 | DISKOS 3450 | (13,440 bytes/track) |
| 05 | DISKOS 7050 | (13,440 bytes/track) |
| 06 | DISKOS 6650 | |
| 07 | DISKOS 15450 | |
| 08-0F | Reserved | |
| 10 | Reserved | |
| 11 | DISKOS 1070-1 | |
| 12 | CD8005 | |
| 13 | CD8010 | |
| 14 | Reserved | |
| 15 | DISKOS 1070-2 | |
| 16-1F | Reserved | |
| 20-FF | Reserved | |

**Table 10.8-1 Status Register Bit Definitions**

| Bit | Name | Description |
|---|---|---|
| 0 | READY | The drive is up to speed, the servo system is locked onto a servo track, and the drive is able to read, write or seek. |
| 1 | SEEK COMPLETE | A seek operation has been completed. This bit is not valid when the BUSY bit is set. |
| 2 | SEEK | A fault was detected during a seek operation. This bit is not valid when the BUSY bit is set. |
| 3 | CYLINDER ZERO | The head carriage is at cylinder zero. This bit is not valid when the BUSY bit is set. |
| 4 | BUSY | The drive is in the process of executing a command. |
| 5 | DRIVE FAULT | A fault was detected during a write operation, or a drive unsafe condition was detected. |
| 6 | WRITE PROTECT | The selected head is write protected. WRITE PROTECT is set by switches on the main PCB. The entire drive is write protected when it is not sequenced up. |
| 7 | COMMAND REJECT | The controller attempted to write to a register when the drive was not READY, or an invalid command was received by the drive. This bit is not valid when the BUSY bit is set. |

**Table 10.8-2 Address Register Bit Definitions**

| Byte | Bit Number 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Upper Byte | 0 | 0 | 0 | 0 | 0 | $C_{10}$ | $C_9$ | $C_8$ |
| Lower Byte | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ |

As indicated in the above table, up to eleven bits of information can be stored in the address registers. This information may be the target cylinder address, the current cylinder address, or the requested parametric information, such as bytes per sector or drive ID. $C_{10}$ is the most significant bit, and $C_0$ is the least significant bit.

## SMD Interface

11.1 **Overview.** PRIAM offers an optional SMD interface, designed to permit PRIAM Winchester disc drives to be used with existing Storage Module Device (SMD) controllers. This interface is available as an SMD *IMBED* with all PRIAM 14-inch disc drives.

Two interface cables are used with the SMD interface — a 60-conductor "A" cable and a 26-conductor "B" cable. Line drivers and receivers in the SMD interface are matched to those of typical SMD controllers.

Two SMD drive characteristics that are not supported by PRIAM drives are the support of address marks and dual porting. Also, PRIAM uses pin numbers 59 and 60 ("A" cable spares) to allow, at the user's option, 11-bit cylinder addresses, whereas 10-bit cylinder addresses are the SMD standard.

Some interface lines have timing characteristics that vary somewhat as a function of the PRIAM drive type. This variation is due to differences in the basic product characteristics. The following lines are affected:

Tag 2
Index
Sector
Seek End
On Cylinder
Return to Zero
Power Sequence Pick
Power Sequence Hold

11.2 **Connectors and Pin Assignments.** Two cables are used for transmitting signals between the disc drive and the controller. One (the "A" cable) contains parallel data, status, Unit Select, and control signals. The other ("B" cable) contains serial data, clocking and sync signals.

A termination resistance is required at the transmitter and receiver end of each transmission line in the "A" cable. This resistance is provided on the drive by an optional terminator assembly which must be ordered separately. A standard SMD termination resistance is required at the controller end of each "A" cable line, except for the Open Cable Detect Line.

A termination resistance (as shown in Section 11.4) is required at the receiver end of each transmission line in the "B" cable. At the disc drive end, this resistance is provided on the SMD interface MAIN PCB.

Characteristics of the required connectors and cables are listed on the following pages.

### I/O Cable Connectors

**"A" Cable**

| Description | Berg Part Number | Spectra Strip Part Number |
|---|---|---|
| Connector (60 pin) | 65043-007 | |
| Contact, insert | 48048 | |
| Flat Cable (twisted Pair) 30 pairs, 28 AWG | | 3CT-6028-7B-05-100 |

**"A" Cable Mating Connector on Drive or Controller**

| Description | AMP Part Number |
|---|---|
| 60 pin right angle header | 3-86479-4 |
| 60 pin vertical header | 3-87227-0 |

**"B" Cable**

| Description | 3M Part Number |
|---|---|
| Connector (26 pin) | 3399-3000 |
| Connector pull tab | 3490-2 |
| Flat cable (26 connector) with ground plane and drain wire | |

**"B" Cable Mating Connector on Drive or Controller**

| Description | AMP Part Number |
|---|---|
| 26 pin right angle header | 1-86479-0 |
| 26 pin vertical header | 1-87227-3 |

### I/O Cable Characteristics

**"A" Cable**

| | |
|---|---|
| Type: | 30 twisted pair, flat cable |
| Twists per inch: | 2 |
| Impedance: | 100 ± 10 ohms |
| Wire size: | 28 AWG, 7 strands |
| Propagation time: | 1.6 to 1.8 ns/foot |
| Maximum cable length: | 100 feet cumulative |
| Voltage rating: | 300 volts rms |

**"B" Cable (With Ground Plane)**

| | |
|---|---|
| Type: | 26 conductor, flat cable with ground plane and drain wire |
| Impedance: | 65 ohms (3M part number 3476-26) |
| Wire size: | 28 AWG, 7 strands |
| Propagation time: | 1.5 to 1.8 ns/foot |
| Maximum cable length: | 50 feet |
| Voltage rating: | 300 volts rms |

**"B" Cable**

| | |
|---|---|
| Type: | Twinax |
| Impedance: | 160 ± 16 ohms |
| Wire size: | 30 AWG, 7 strands |
| Diameter over outer insulator: | 0.620" maximum |
| Propagation velocity: | 70% minimum |
| Maximum cable length: | 50 feet |

11.3 **Interface Signal Descriptions.** This section gives functional descriptions for the signals on the "A" and "B" Interface connectors.

Address and control information is transferred to the drive on a 10-bit bus, with three tag lines defining the type of information on the bus. Unit selection is provided by four binary coded lines gated into the drive by a Unit Select tag. Major status conditions of the selected drive, as well as index and sector marks, are returned to the controller on seven lines.

Data and clock signals between the drive and the controller require five lines. These lines are associated with a physical drive using a radial connection between the drive and the controller. Two additional lines in this cable supply an interrupt signal (Seek End) and an indication of selection (Unit Selected). See Tables 11.2-1 and 11.2-3 for the pin assignments of these lines on the two interface cables.

Table 11.2-1. Tag Bus I/O Interface ("A" Cable)

| Function | Connector Pins Low | High | Connector Pin Layout | |
|---|---|---|---|---|
| Unit Select Tag | 43 | 44 | 2 | 1* |
| Unit Select $2^0$ | 45 | 46 | 4 | 3 |
| Unit Select $2^1$ | 47 | 48 | 6 | 5 |
| Unit Select $2^2$ | 51 | 52 | 8 | 7 |
| Unit Select $2^3$ | 53 | 54 | 10 | 9 |
| Tag 1 | 1 | 2 | 12 | 11 |
| Tag 2 | 3 | 4 | 14 | 13 |
| Tag 3 | 5 | 6 | 16 | 15 |
| Bit 0 | 7 | 8 | 18 | 17 |
| Bit 1 | 9 | 10 | 20 | 19 |
| Bit 2 | 11 | 12 | 22 | 21 |
| Bit 3 | 13 | 14 | 24 | 23 |
| Bit 4 | 15 | 16 | 26 | 25 |
| Bit 5 | 17 | 18 | 28 | 27 |
| Bit 6 | 19 | 20 | 30 | 29 |
| Bit 7 | 21 | 22 | 32 | 31 |
| Bit 8 | 23 | 24 | 34 | 33 |
| Bit 9 | 25 | 26 | 36 | 35 |
| Open Cable Detector | 27 | 28 | 38 | 37 |
| Index | 35 | 36 | 40 | 39 |
| Sector | 49 | 50 | 42 | 41 |
| Fault | 29 | 30 | 44 | 43 |
| Seek Error | 31 | 32 | 46 | 45 |
| On Cylinder | 33 | 34 | 48 | 47 |
| Unit Ready | 37 | 38 | 50 | 49 |
| Unused (always 0) | 39 | 40 | 52 | 51 |
| Write Protected | 55 | 56 | 54 | 53 |
| Power Sequence Pick | | 57 | 56 | 55 |
| Power Sequence Hold | | 58 | 58 | 57 |
| Unused | 41 | 42 | 60 | 59 |
| Spare (Optional Bus Bit 10) | 59 | 60 | | |

* = Triangle Mark

60 position, 28 AWG, 30 twisted pair
straight flat cables
maximum length -- 100 feet

**Table II.2-2 Tag Bus Decode ("A" Cable)**

| Bus | Tag 1 Cylinder Address | Tag 2 HEAD Select | Tag 3 Control Select |
|---|---|---|---|
| Bit 0 | $2^0$ | $2^0$ | Write Gate |
| Bit 1 | $2^1$ | $2^1$ | Read Gate |
| Bit 2 | $2^2$ | $2^2$ | Unused |
| Bit 3 | $2^3$ | Unused | Unused |
| Bit 4 | $2^4$ | Unused | Fault Clear |
| Bit 5 | $2^5$ | Unused | Unused |
| Bit 6 | $2^6$ | Unused | RTZ |
| Bit 7 | $2^7$ | Unused | Unused |
| Bit 8 | $2^8$ | Unused | Unused |
| Bit 9 | $2^9$ | Unused | Unused |
| Bit 10 (optional) | $2^{10}$ | Unused | Unused |

**Table II.2-3 "B" Cable Interface.**

| Function | Connector Pins Low | Connector Pins High | Connector Pin Layout |
|---|---|---|---|
| Write Data | 15 | 14 | 2 1Δ |
| Ground | | 13 | 4 3 |
| Write Clock | 11 | 12 | 6 5 |
| Ground | | 10 | 8 7 |
| Servo Clock | 3 | 2 | 10 9 |
| Ground | | 1 | 12 11 |
| Read Data | 5 | 6 | 14 13 |
| Ground | | 4 | 16 15 |
| Read Clock | 9 | 8 | 18 17 |
| Ground | | 7 | 20 19 |
| Seek End | 19 | 20 | 22 21 |
| Unit Selected | 18 | 17 | 24 23 |
| Ground | | 16 | 26 25 |
| Index | 23 | 22 | |
| Ground | | 21 | |
| Sector | 25 | 26 | |
| Ground | | 24 | |

26 connector flat cable
maximum length — 50 feet

1. The 10 bus lines are used to transmit cylinder address, head address, or control functions from the controller to the drive. Bit 0 is the least significant bit, and Bit 9 is the most significant bit (unless Bit 10 is used).

   If the optional Bus Bit 10 is used, Bit 10 is the most significant bit. The normally spare pair, pins 59 and 60 of "A" Cable, is used for this purpose. This bit is enabled:

   6650SMD W16 in A-B Position
   15450SMD W4 in A-B Position

2. *Tag 1 (Cylinder Address)* When Tag 1 is active, the ten (or eleven) bus lines are used to carry the cylinder address to the drive. Since the drive is a direct addressing device, the controller need only place the new address on the lines and strobe the lines with Tag 1 (see Figure *II.5-1*). The drive must be On Cylinder before Tag 1 is sent. The bus lines should be stable throughout the tag time.

3. *Tag 2 (Head Select)* When Tag 2 is active, the bus bit lines are used to carry the head address information to the drive. The controller places the head addresses on the lines with Tag 2.
   In the 3350-20 and 6650-20, only bus bits 0 and 1 are used. In the 15450-20 bus bits 0, 1, and 2 are used.

4. *Tag 3 (Control Select)* Tag 3 acts as an enable, and must be true for the entire control operation (see Table *II.2-2*).

   a. Bit 0 (Write Gate)

      Write Gate enables the write driver. See Figure *II.5-4* for typical Write Gate timing requirements.

      *NOTE:* Write Gate to Read Gate timing is 14 microseconds (see Figure *II.5-4*) instead of the 10 microseconds required by the standard SMD specification.

   b. Bit 1 (Read Gate)

      Read Gate enables digital read data onto the Read Data lines. The leading edge of Read Gate triggers the read chain to synchronize on an all zeros pattern (see Figures *II.5-2*, *II.5-3*, and *II.5-4* for typical Read Gate timing).

      *NOTE:* Write Gate to Read Gate timing is 14 microseconds (see Figure *II.5-4*) instead of the 10 microseconds required by the standard SMD specification.

   c. Bit 2 (Servo Offset Plus)

      In all drives using the SMD adapter, this function is not supported, and no response will occur when this operation is attempted.

   d. Bit 3 (Servo Offset Minus)

      In all drives using the SMD adapter, this function is not supported, and no response will occur when this operation is attempted.

e. Bit 4 (Fault Clear)

This line clears Fault status. The Fault status may recur if the fault condition still exists.

f. Bit 5 (AM Enable)

Not supported by this interface. No response will occur when this operation is attempted.

g. Bit 6 (RTZ)

This line moves the head carriage to cylinder zero, sets the head address to head zero, and clears Seek Error.

h. Bit 7 (Data Strobe Early)

Not supported by this interface. No response will occur when this operation is attempted.

i. Bit 8 (Data Strobe Late)

Not supported by this interface. No response will occur when this operation is attempted.

j. Bit 9 (Release)

Not supported by this interface. No response will occur when this operation is attempted.

5. *Unit Select Tag* Unit Select Tag is used to select the drive defined by the Unit Select 1, 2, 4 and 8 lines. The drive is selected at the leading edge of Unit Select Tag, and responds (within 200 nanoseconds) with Unit Selected. The drive address on the Unit Select lines must be stable 200 nanoseconds before the leading edge of Unit Select Tag.

In all drives using the SMD adapter, the Unit Select Tag must remain stable throughout the time that the drive is selected. For detailed timing information, see Figure *II.5-6*

6. *Unit Select 1, 2, 4 and 8* These four lines are binary coded to select one of 16 logical drive addresses. The address placed on the Unit Select lines is compared by each drive against the logical address determined by the settings of the drive address switches on the main PCB. When the Unit Select Tag rises, the drive which compares equal becomes the one selected. Care must be taken to assure that each physical drive is assigned a different logical address.

Four dip switches are used for assigning the drive a logical address at installation time, or at any subsequent time.

7. *Individual Lines*

a. Sector

The sector mark is derived from the servo track data, using a byte counter. Timing integrity is maintained throughout seek operations (see Figure *II.5-5*). The number of sectors per revolution and/or the number of bytes per sector, is switch selectable. In the *14" disk drives*, the sector switches are located on the *MAIN or SPLIT* PCB. See the INSTALLATION section for specific information on switch settings.

The microprocessor sets sector size during initialization. If the switch settings are changed while the drive is powered up, power must be removed from the drive and then restored to cause the newly selected sector size to be established at the drive.

b. Fault

When the Fault Line is true, a fault condition exists at the drive. The drive can detect the following types of faults:

1. Write Fault (Write Gate with Write Protect)
2. Write Off Cylinder (Write Gate without On Cylinder)
3. Multiple Heads Selected
4. No transitions during write (MFM format)
5. Write Gate without write current at the head
6. Write current at the head without Write Gate
7. Write when servo is off track
8. Write during a Servo Offset operation
9. Write Gate and Read Gate occurring simultaneously
10. Read Off Cylinder (Read Gate without On Cylinder)
11. Unable to Restore (RTZ) drive

A Fault condition immediately inhibits writing. The Fault line may be reset by Fault Clear, or by Restore (RTZ).

c. *Seek Error* When the Seek Error line is true, a seek error has occurred. The Seek Error line may be reset by RTZ. Seek Error indicates that the drive was unable to complete a seek operation. When this condition is detected, the drive automatically returns to cylinder zero.

*Note:* For 3350s a seek address greater than 560 (230 hex), or for 6650, 15450, address greater than 1120 (460 hex) will cause Seek Error to go true within 450 microseconds, instead of the 100 nanoseconds required by the standard SMD specification.

d. On Cylinder

On Cylinder indicates that the servo has positioned the heads over the desired data tracks. On Cylinder is reset by a Seek operation or a Restore operation.

e. Index

The Index signal occurs once per revolution. Its leading edge is considered the leading edge of Sector Zero. Index is typically a two-byte wide pulse (see Figure 11.5-5). Timing integrity is maintained throughout seek operations.

f. Unit Ready

Unit Ready indicates that the drive is up to speed, the heads are positioned over the recording surface, and no fault condition exists.

g. Open Cable Detector

Open Cable Detector must be false to Gate the select bits into the compare circuitry.

The open cable detect circuit disables the interface whenever the "A" Cable is disconnected.

h. Address Mark Found

Address Mark Found is not supported by this interface. This line is always false.

i. Unit Selected

When the four Unit Select lines compare with the setting of the drive address switches on the SMD Board and the Unit Select Tag is active, the Unit Selected line on the "B" Cable goes true (see Figure 11.5-6). If, on a multi-drive system, multiple Unit Selected responses are received by the controller, it may indicate that duplicate switch settings have been used.

j. Write Protected

Setting the Write Protect switch on the drive's Main or Split PCB inhibits all write operations, and causes the Write Protected line to be true.

Attempting to write to a protected drive will cause the Fault line to go true.

k. Seek End

Seek End is the OR combination of On Cylinder or Seek Error. It indicates that a seek operation has terminated (see Figure 11.5-1 for timing details).

l. Power Sequencing

Power Sequencing is not supported by this interface. Power Sequence Pick and Power Sequence Hold are interconnected to represent a Sequenced Up drive at all times.

Both Power Sequence Pick and Power Sequence Hold must be held at ground potential to enable drive operation. If either line is open, or at +1.4 volts or greater, the drive will sequence down (move the heads to the landing zone and stop the spindle motor) and remain sequenced down until both lines are again at ground potential. When this occurs, the drive will sequence up and, when the motor is at speed, become Ready.

m. Busy

The Busy indication is not supported by this interface.

8. *Data and Clock Lines* (see Figure 11.5-7)

a. Write Data

The Write Data Lines carry NRZ data to be recorded on the disc.

b. Servo Clock

The Servo Clock is a phased-locked clock generated from the servo track data. It is used to synchronize write data. Servo Clock is available at all times (not gated by Unit Select) that the drive is Ready.

c. Read Data

The Read Data lines transmit the recovered data in NRZ form.

d. Read Clock

The Read Clock signal defines the beginning of data bit cell. Read Clock is an internally

derived clock signal that is synchronous with the recovered data, as shown in Figure 11.5-7. Read Clock is in phase sync with the Read Data within 8 microseconds after the leading edge of Read Gate.

e. Write Clock

The Write Clock signal from the controller to the drive must be synchronized with the NRZ write data, as shown in Figure 11.5-7. The Write Clock is the Servo Clock retransmitted to the drive during a write operation. Write Clock need not be transmitted continuously, but must be transmitted during, and at least 250 nanoseconds prior to Write Gate.

11.4 **Interface DC Characteristics.** This section, through tables and figures, sets forth the details that need to be observed in order to properly transmit and receive the interface signals.

All input and output signals are digital, using SMD standard transmitters and receivers to provide a terminated, balanced transmission system.

The "A" cable is a twisted pair flat cable. The "B" cable is a flat ribbon cable with ground plane and drain wire. Twisted pair or ground plane shielding, or both, are used to minimize crosstalk and to reduce inductive coupling.

1. *Terminated and Balanced Transmission System* Transmitters and receivers of the SMD standard types 75110A and 75108 or equivalent are used to provide a terminated and balanced transmission system, as shown in Figure 11.4-1.

*Terminating resistors are on adapter logic card or controller. These signals must be star cabled.

2. *Line Transmitter Characteristics* The SMD standard line transmitters (Figure 11.4-2) are compatible with the line receivers described below.

a. Output Signal Levels

Data Signals: see Figure 11.4-1.
Control Signals: see Figure 11.4-2.

b. Output Line Polarity

Control Signals: On the "A" Cable, the transmitters are connected to the I/O line so that the output, labeled Z (Figure 11.4-2) is connected to the odd numbered pin of the cable connector. This output in turn connects to the receiver pin labeled B (Figure 11.4-3) except for the Unit Selected line, which is connected in the opposite manner.

When transmitter and receiver are connected in this manner, a logical 1 into the transmitter produces a logical 1 out of the receiver,

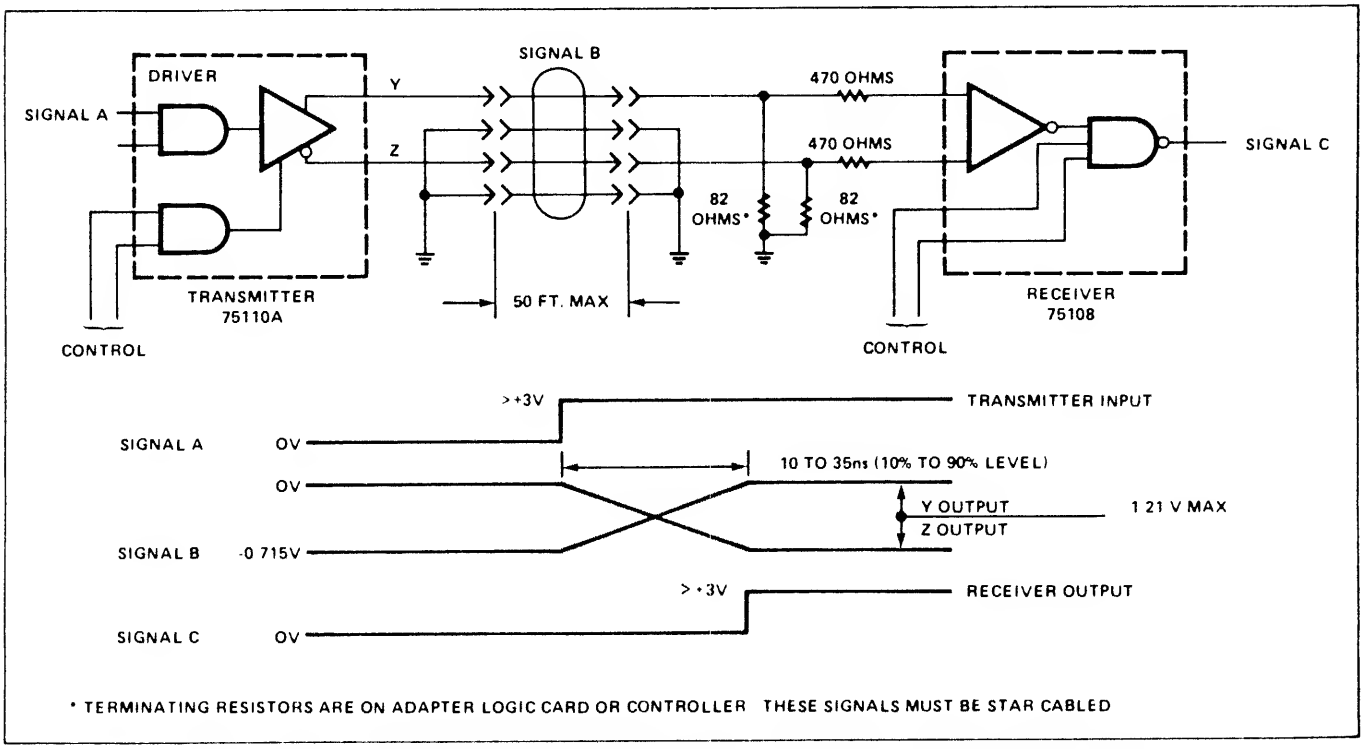



**Figure 11.4-1 Typical Read/Write Data and Clock Transmitter and Receiver**

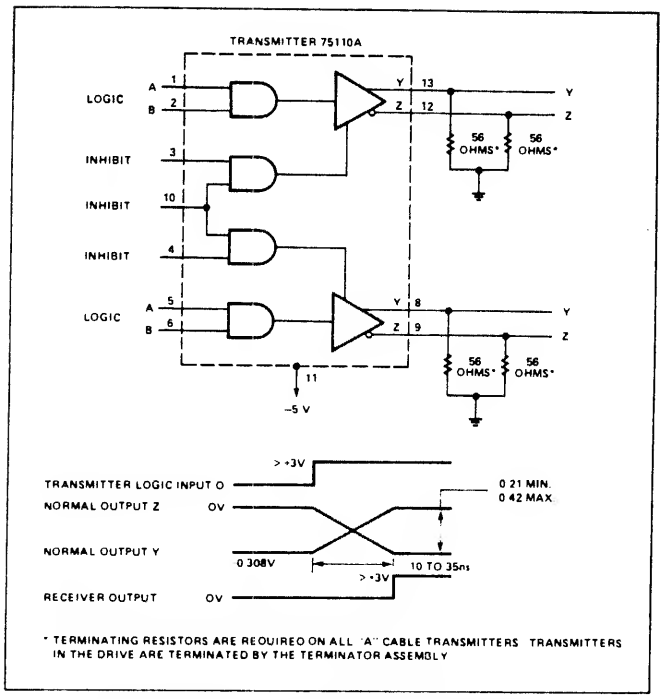



**Figure 11.4-2 Control Line Transmitter**

except for the Unit Selected line, where a logical 1 into the transmitter produces a logical 0 out of the receiver.

3. *Input Amplifier (Receiver) Characteristics* The drive's input amplifier (Figure 11.4-3) is SMD-standard compatible with the line transmitter described above.

a. Receiver Propagation Delay

The receiver propagation delay is typically 17 nanoseconds, both for a logical 0-to-1 transition and for a logical 1-to-0 transition.

b. Receiver Input Polarity

Control Signals: The input, labeled B (Figure 11.4-3) of the receiver is connected to the odd numbered pin of the cable connector, and thus connects to the transmitter pin labeled Z (Figure 11.4-2).

Data Signals: see Figure 11.4-1

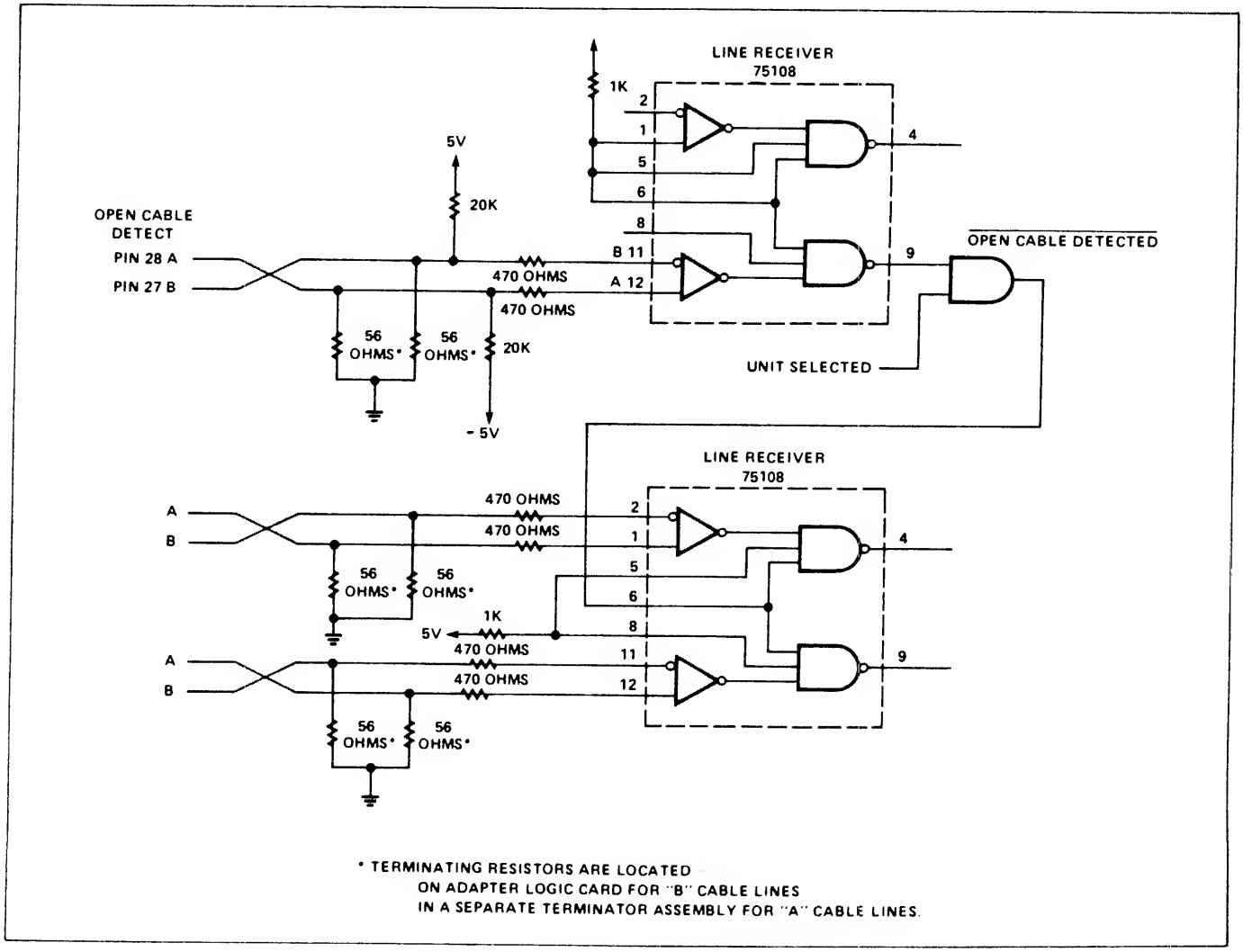
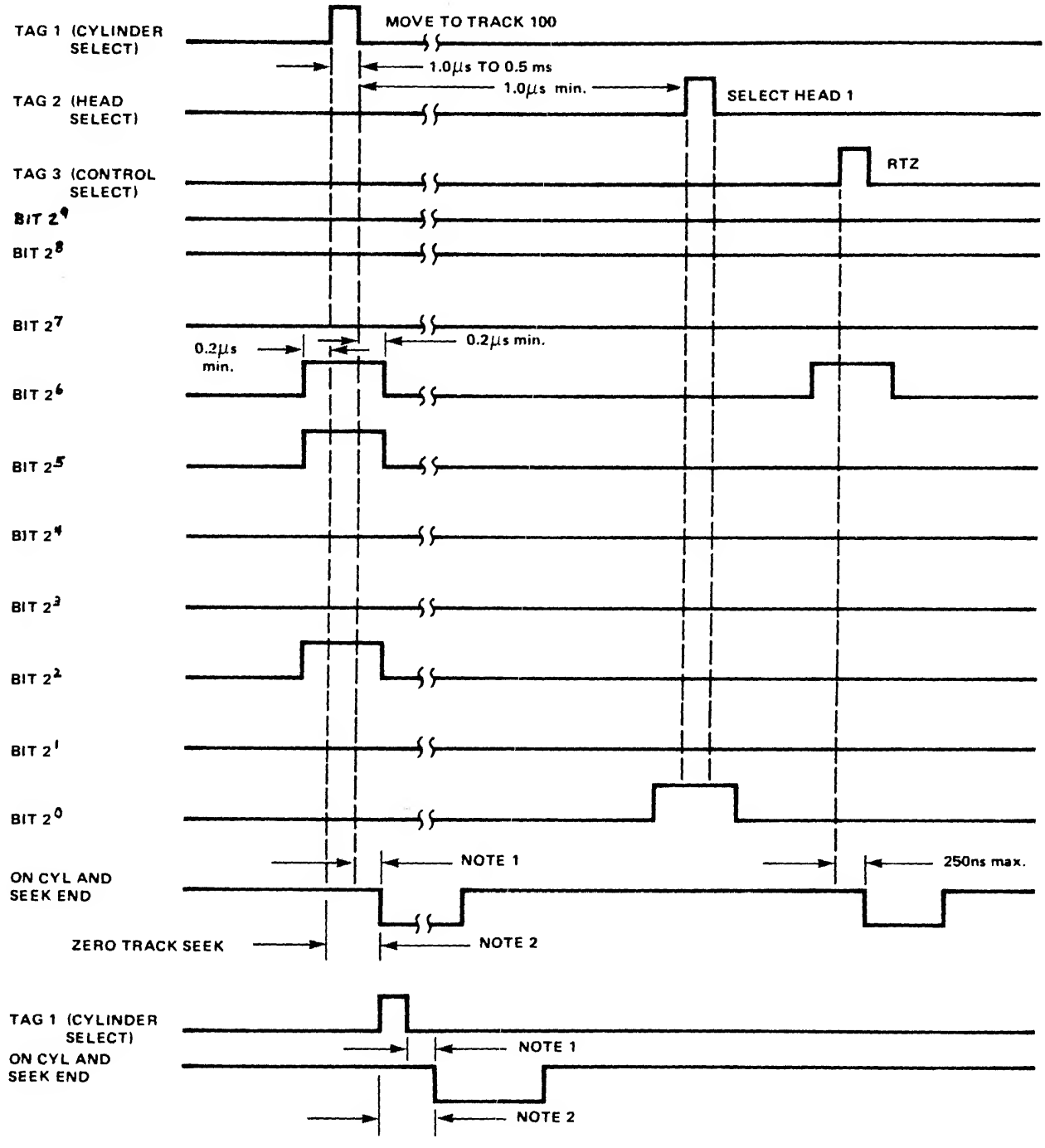



**Figure 11.4-3 Control Line Receiver**

11.5 **Interface Timing.** This section discusses the timing requirements for the various operations performed on the controller interface.

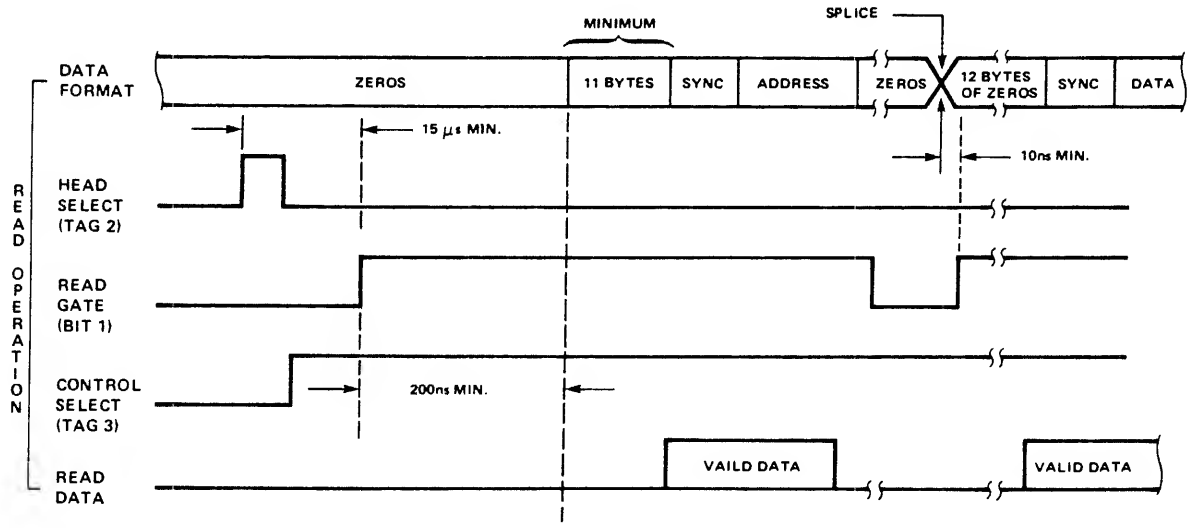



NOTE 1: 120 ns MAXIMUM FOR 3350 SMD, 6650 SMD, AND 15450 SMD (14" DRIVES WITH IMBEDDED SMD INTERFACE). SEE NOTE 2 FOR ALL OTHER DRIVES.

NOTE 2: 450 ns FROM LEADING EDGE OF TAG 1 FOR ALL DRIVES USING SMD ADAPTER.

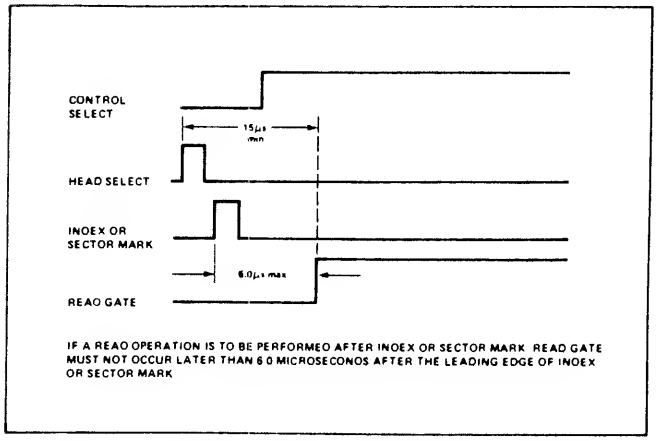
ON CYLINDER AND SEEK END SIGNALS ARE IDENTICAL UNLESS A SEEK ERROR OCCURS. SEEK ERROR INITIATES A CONSTANT SEEK END UNTIL RTZ CLEARS THE ERROR.

**Figure 11.5-1 Tag and Bus Timing**




READ GATE MUST BE DROPPED PRIOR TO THE WRITE SPLICE. IT MUST BE RAISED AT LEAST ONE BIT AFTER THE WRITE SPLICE, AND WITH AT LEAST 10 BYTES OF ZEROS REMAINING IN THE SYNC FIELD. A 12-BYTE EXAMPLE CONSISTS OF ONE BYTE FOR WRITE SPLICE AND 11 BYTES FOR VFO SYNC.

**Figure 11.5-2 Typical Read Timing**




IF A READ OPERATION IS TO BE PERFORMED AFTER INDEX OR SECTOR MARK READ GATE MUST NOT OCCUR LATER THAN 6.0 MICROSECONDS AFTER THE LEADING EDGE OF INDEX OR SECTOR MARK

**Figure 11.5-3 Typical Read Control Timing**

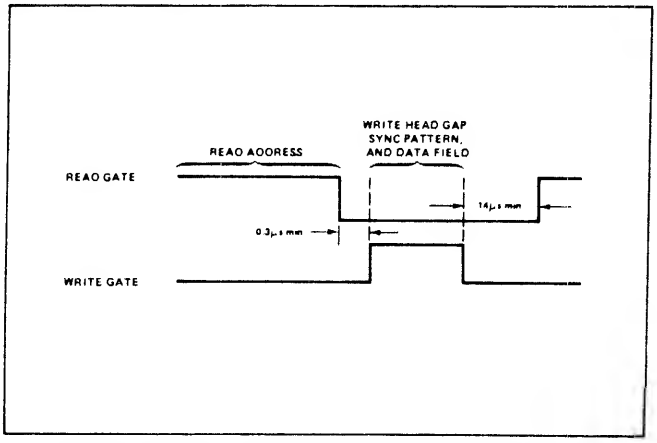
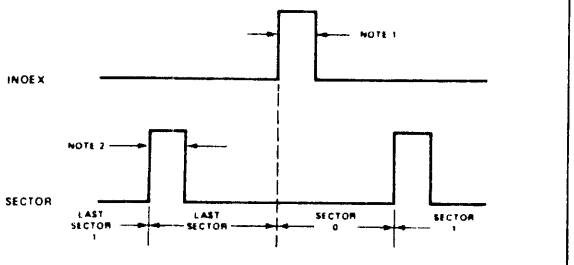



**Figure 11.5-4 Typical Write Control Timing**




Note 1: 1.92us for 14 inch SMD
Note 2: 960 ns for 14 inch SMD

**Figure 11.5-5 Index and Sector Mark**

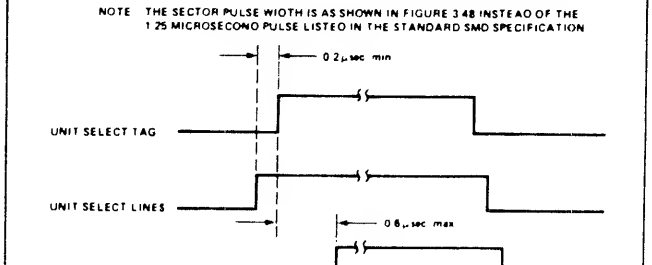
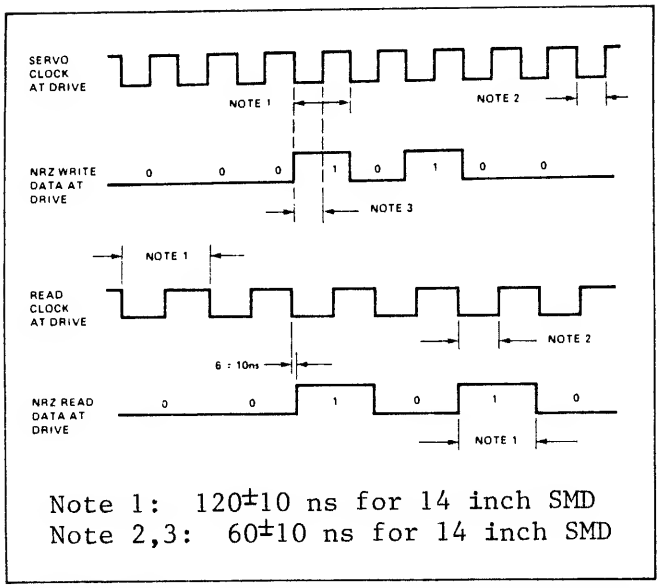



**Figure 11.5-6 Drive Select Timing**




Note 1: 120±10 ns for 14 inch SMD
Note 2,3: 60±10 ns for 14 inch SMD

**Figure 11.5-7 NRZ Data and Read Clock Timing**

11.6 **Format Design.** Some hardware oriented constraints must be observed when designing a format. The following is a list of the parameters involved:

a. *Read Initialization Time* Between the deselection of one head and the selection of another head, there is a 5-microsecond delay within the drive, due to circuit characteristics. The time from the initiation of a head change until data can be read using the selected head is 24 microseconds maximum (5 microseconds for head selection, 10 microseconds for read amplifier stabilization, and 9 microseconds for phase lock synchronization).

b. *Write-to-Read Recovery Time* Assuming head selection is stabilized, the time before Read Gate can be enabled after switching Write Gate off is 10 microseconds minimum.

c. *Read-to-Write Recovery Time* Assuming head selection is stabilized, the time before Write Gate can be enabled after switching Read Gate off is 1.0 microsecond minimum.

d. *Beginning-of-Record Tolerance* This tolerance (a gap of 9 bytes) allows for write splice and write-to-read recovery time for multisector operations (see Figure 11.6-1).

e. *Read VFO Synchronization* 8 microseconds are needed for the variable frequency oscillator to synchronize. Zeros should be written during this time.

f. *Sync Pattern* The sync pattern, indicating the beginning of the address or data area, consists of 1 byte.

g. *Write Driver Turn On* The write driver turn on time is about 960 nanoseconds (one byte time). This time must be accounted for, in order to know where the splice areas are located.

11.7 **Write Format Procedure.** Provision must be made to format the disc. A suggested format is shown in Figure 11.6-1 The following procedure is recommended:

a. Select desired drive, cylinder, head, and sector.

b. The controller must provide a 5 microsecond minimum delay after selecting a head before starting a search for the leading edge of the sector pulse is detected.

c. Search for leading edge of desired sector.

d. Detect leading edge of the desired sector and raise Write Gate.

e. Write all zeros for write recovery and VFO sync field (20 bytes minimum).

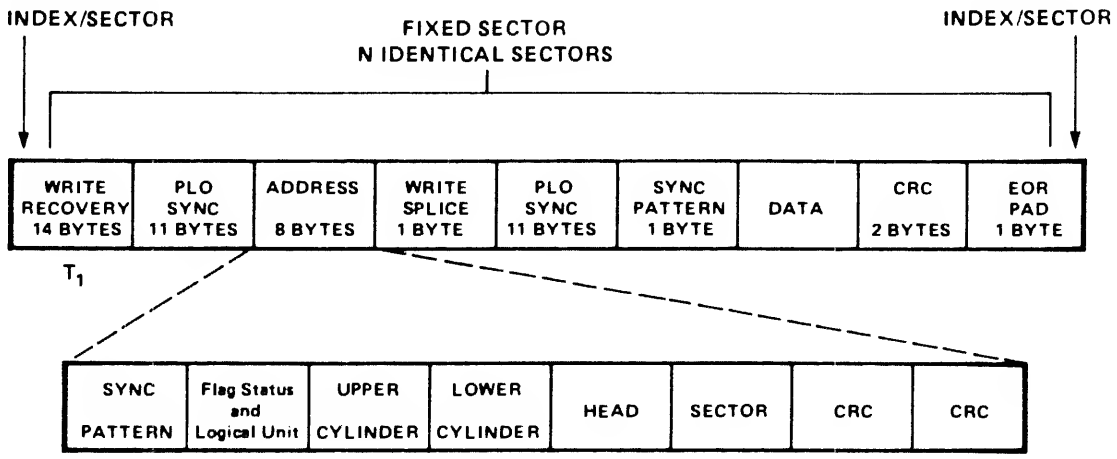
f. Write a sync pattern, the address, and the address checkword.

g. Write all zeros for write splice gap and VFO sync field (12 bytes minimum).

h. Write a sync pattern, the data field, the two-byte data field checkword, and the five-byte field of zeros (see Figure 11.6-1). The data field should preferably be a worst case pattern.

i. The end tolerance gap specified by the standard SMD specification is not required by this drive. However, if it is used, it is recommended that zeros be written to the next sector pulse.

j. If the next sector of the same track is to be formatted, and the head is not deselected, Write Gate should be left on. In this case, all zeros should be written until the leading edge of the next sector or index pulse.




$T_1$ = TIME BETWEEN LEADING EDGE OF INDEX/SECTOR AND READ GATE. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

EXAMPLE: WHAT IS THE DATA FIELD LENGTH USING 66 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - \text{(SYNC FIELDS, TOLERANCE, GAPS AND ADDRESSES)}$$

$$= \frac{20{,}160^*}{66} - 49 = 256 \text{ BYTES/SECTOR}$$

$$\%\ \text{EFFICIENCY} = \frac{256 \times 66}{20{,}160} \times 100 = 83.8\%$$

* 20,160 BYTES/TRACK ASSUMED.

NOTE: WRITE RECOVERY IS 14 BYTES INSTEAD OF 16 BYTES, AND EOR PAD IS 1 BYTE INSTEAD OF 8 BYTES, AS RECOMMENDED BY THE STANDARD SMD SPECIFICATION.

**Figure 11.6-1 Recommended Sector Format**

## 11.8 Control Timing.

a. Read Data Field

Read Gate is the control line associated with a read operation.

The leading edge of Read Gate allows the VFO to synchronize on all-zeros pattern. Read Gate also enables the output of the data separator onto the I/O lines. There may be invalid data transitions on these lines during the synchronization period. Read Gate must be dropped and raised again after going through a splice area. Read Gate may be enabled 60 ± 4 clock periods after the leading edge of index or sector.

The sync pattern search may begin 72 servo clock periods (9 byte times) after the leading edge of Read Gate.

Head switching and read amplifier stabilization requirements (Figure 11.6-1) determine the latest time at which a head can be selected, in order to read the next successive sector, using the format shown in Figure

Read Data and Read Clock may not have valid data until 8 microseconds after the leading edge of Read Gate, due to the VFO synchronizing time.

There should be no splice area while Read Gate is raised.

b. Write Data Field

Write Gate is the control line associated with a write operation.

The sector address must always be read and verified, prior to writing the data field, except while formatting.

Writing the data field must always be preceded by writing the VFO sync field and sync pattern.

The controller must provide an internal delay of at least two bit times (approximately 240 nanoseconds) between the trailing edge of Read Gate and the leading edge of Write Gate. This delay allows for signal propagation tolerances and prevents overlap of Read Gate and Write Gate in the drive.

Writing the data field must always be followed by writing the data checkword and at least an eight-bit gap of zeros at the end of the checkword.

During formatting, Write Gate is raised upon detecting index or sector. During a record update, Write Gate is raised within two byte times after the last bit of the address.

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